EMR

720-02

GENERAL INFORMATION

BIT SYNCHRONIZER

FOX RIVER BOND
25% COTTON

GENERAL INFORMATION

GENERAL
INFORMATION

INSTRUCTION MANUAL

EMR MODEL 720-02

BIT SYNCHRONIZER

(REVISION E)

38077

SANGAMO WESTON
Schlumberger

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains information describing the EMR Model 720-02 Bit Synchronizer. Included in this information is a functional and physical description, specifications, and installation and operation instructions.

1.2 FUNCTIONAL DESCRIPTION

The bit synchronizer accepts serial PCM data in the presence of noise and other perturbations and generates reconstructed coherent PCM data and timing signals. The 720 can process all standard Inter-Range Instrumentation Group (IRIG) PCM codes which include NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, RZ, DM-M and DM-S. The unit accepts inputs over the bit range of 1 bit-per-second (bps) to 5 megabits-per-second (Mbps) for these codes.

The 720 can be programmed either by front-panel controls or by a computer. Manual operation is provided by front-panel pushbutton and thumbwheel controls. In remote programming operation, the program setup is displayed with alphanumeric characters and solid-state indicators located directly above the functional pushbutton controls. A double memory retains the parameters set up by either the front-panel switches or by remote programming. For quick modification of the stored remote program, an override control provides access to the stored program. The operating program control lines are brought out to rear-panel connectors for monitoring.

The 720's input filter is a matched filter to square PCM signals. This filter provides the response of a reset integrator for square-wave (unfiltered) inputs, but is free from the transient and timing errors inherent in switching reset integrators at high bit rates. This filter also provides a nearly optimum linear phase response characteristic for processing premodulation-filtered signals.

A highly stablized VCO is incorporated in the bit synchronization phase-locked loop whose nominal center frequency is controlled by a frequency synthesizer consisting of programmable digital dividers and a precision, low-frequency reference oscillator. A dual phase detector provides fast BiØ ambiguity resolution.

All digital logic circuits use medium scale integrated (MSI) logic elements. The use of solid-state switches and light-emitting diode indicators further ensures unit reliability.

The 720 contains an internal power supply (with line filter), regulator, and cooling facilities. The internal power supply operates from an AC power source to generate all voltages necessary for operation of the bit synchronizer.

1.3 PHYSICAL DESCRIPTION

The bit synchronizer is a self-contained unit, 21-1/2 inches in overall depth (excluding rear-mounted connections and front-panel projections), designed for mounting in a standard 19-inch rack or portable instrument case. The unit is 5-1/4 inches high and occupies 19 inches of panel width in the mounting equipment. The major subassemblies of the bit synchronizer are illustrated in Figure 5-1 and described in Table 1-1.

Table 1-1. Model 720 Bit Synchronizer, List of Major Subassemblies (Ref. Figure 5-1)

REF. DESIG.	NAME	DESCRIPTION
A1	Interconnection Printed-Wiring Assembly (Motherboard)	Contains mating connectors for all printed-circuit cards and contains interconnection wiring between subassemblies of the bit synchronizer. Also contains TRACKING RANGE, INPUT PCM, DATA POLARITY, and INPUT CODE switch assemblies.
A2	Front Subpanel Assembly	Contains controls, indicators, and monitor jacks used in the operation of the bit synchronizer. This assembly plugs into J14 on Interconnection Assembly A1. A description of the front-panel components is contained in Table 3-6.
A3	Right Side Panel Assembly	Contains power supply components (heatsink assembly, transformer T1, etc.).
A4	Rear Panel Assembly	Contains (1) connectors for termination of all wiring between bit synchronizer and peripheral equipment; (2) blower; (3) elapsed time meter; and (4) primary power line filters FL1 and FL2.
Printed-Wiring Assy. (PWA) at A1J1	Source Select (Card 1)	Contains the following circuits: (1) circuit for selecting one of four input sources; (2) AGC circuit; (3) input voltage status (overvoltage or undervoltage) circuits; and (4) circuit that detects loss of PCM input and turns on SIGNAL LOSS lamp.
PWA at A1J2	Input Filter, First Pole Pair (Card 2)	First pole-pair of input filter that can accept either square PCM or filtered PCM inputs.
PWA at A1J3	Input Filter, Second Pole Pair (Card 3)	Second pole-pair of input filter and filter-summing amplifiers.

Table 1-1 (Cont'd.). Model 720 Bit Synchronizer, List of Major Subassemblies (Ref. Figure 5-1)

REF. DESIG.	NAME	DESCRIPTION
PWA at A1J4	Filter Control (Card 4)	Controls the tuning of the input filter, derives internal timing signals from the filtered input signal, and provides suitable delays in the filtered PCM signal to optimize performance at the high bit rates.
PWA at A1J5	Loop Filter (Card 5)	Phase-locked-loop filter.
PWA at A1J6	VCO (Card 6)	Phase-locked-loop VCO.
PWA at A1J7	Bit Rate Store (Card 7)	Static stores for storing bit rate selection.
PWA at A1J8	Format Store (Card 8)	Static stores for all operating parameters except bit rate selection.
PWA at A1J9	DC Restorer (Card 9)	After the input PCM signal is filtered, the DC restorer establishes a median operating level upon which the PCM signal is centered.
PWA at A1J10	Code Converter (Card 10)	Converts selected PCM input code to NRZ-L, BiØ-L, and DM output codes. Determines the "sync" status of the unit.
PWA at A1J11	Output Amplifier (Card 11)	Buffers the NRZ-L, BiØ-L, DM, and clock outputs for routing to external equipment.
PWA at A1J13	Regulator (Card 13)	The regulator card (and power supply components mounted on Right Side Panel Assembly A3) operate from a primary AC power input to generate the DC voltages (-18V, +18V, and +5V) required for bit synchronizer operation.

SECTION 2

SPECIFICATIONS

2.1 GENERAL

This section contains the electrical, mechanical, and environmental specifications for the Model 720 Bit Synchronizer. Figure 2-1 illustrates and defines the PCM input codes that can be processed by the bit synchronizer. Figures 2-2 through 2-7 illustrate bit synchronizer performance under various input conditions. Tables 2-1 through 2-3 provide additional specification data. Table 2-4 provides model number identification data, and Table 2-5 contains definitions to clarify the terms used in the specification.

2.2 ELECTRICAL SPECIFICATIONS

2.2.1 Signal Inputs

a. Source: Up to four input sources.

b. Source Isolation: Isolation between channels is better than 40 dB with 100 Ω source impedances.

c. Configuration: Each input single-ended, referenced to signal ground. The input is AC coupled except when operating in NRZ or RZ codes at bit rates less than 100 bps. In these cases, DC coupling is provided by bypassing the input coupling capacitor.

d. Polarity: Each input accepts signals of either polarity or signals symmetrical about signal ground.

e. Level: 0.5V to 30V peak-to-peak without adjustment.

f. Impedance: For all bit rates, 10 kΩ or greater shunted by less than 150 pF. [Provisions are available on the input card to permit impedance matching by the addition of 1 watt resistors (4 required for the 4 inputs.)]

g. Maximum Input Voltage: Up to ±60V peak when non-terminated at the input. When an input terminating resistor is used, the maximum input voltage is further limited by the average power dissipated in the terminating resistor. This power must not exceed 1 watt.

h. Codes: NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, RZ, DM-M and DM-S as defined in Figure 2-1.

i. Tunable Bit Rate: Tunable from 1 bps to 5.000 Mbps.

j. Tuning Resolution: ±.05% of any bit rate by means of front panel or remote control.

k. DC Baseline Offset:

1. With the input AC coupled, the DC offset shall not cause violation of the maximum peak input voltage requirement [refer to (g) on the preceding page].

2. With the input DC coupled [refer to (c) on the preceding page] the amplitude of the DC offset shall not exceed 50% of the peak-to-peak signal amplitude. DC offset plus peak signal not to exceed ± 15 volts.

l. Baseline Variation:

1. With the input AC coupled, the input signal baseline may be shifted by a superimposed sine waveform whose peak-to-peak amplitude is equal to the peak-to-peak amplitude of the PCM wavetrain, and whose frequency is up to 0.1% of the input bit rate. A baseline variation of smaller amplitude and higher rate can also be accepted without degrading the bit error performance.

2. With the input DC coupled, the allowable peak-to-peak amplitude of the sine waveform specified above must be reduced by any DC baseline offset present.

2.2.2 Synchronization

a. Acquisition Time: When processing random NRZ or BiØ data with 50% transition density and a signal-to-noise ratio (SNR) of ≥15 dB, and with the 1.0% loop width selected, the 720 will synchronize to an incoming bit rate which is within ± 2% of the selected bit rate within 100 bit periods, and will synchronize to an incoming bit rate which is within ± 5% of the selected bit rate within 200 bit periods. Refer to Figure 2-2 for typical acquisition performance of the 720.

b. Loop Bandwidth and Tracking Range: For bit rates 10 bps and above, the 720 provides the following three loop widths and associated tracking ranges (expressed in percent of bit rate):

Loop Width	Tracking Range
0.1%	1.0%
0.3%	3.0%
1.0%	10%

For bit rates below 10 bps, only the 1.0% loop width with a 10% tracking range is provided.

c. Loop Stability:

1. Under no-signal (input grounded) conditions, the 720 maintains its internal clock frequency within ±0.5% of the selected bit rate.

2. With white noise only input to the 720, the internal clock frequency will remain within the tracking range related to the selected loop width.

d. Bi-Phase Ambiguity: In bi-phase codes at bit rates below 2.5 Mbps, the 720 will hold frequency lock with a stable incoming bit stream for SNR ≥ 6 dB, regardless of data intelligence. The 720 will resolve bi-phase ambiguity within 200 bits of random "ones" and "zeros" and will maintain the phase resolution for 2000 bits of constant "ones" or "zeros", for SNR ≥ 12 dB.

e. Maintaining Synchronization:

1. With wideband Gaussian noise only, narrow loop width, and 50% transition density, the 720 will maintain synchronization thresholds as shown in Table 2-1.

2. With NRZ codes for SNR ≥ 6 dB, and random data input, the 720 will maintain synchronization under the following adverse conditions.

(a) With baseline perturbations specified in paragraph 2.2.1 (k) and (l).

(b) With amplitude modulation of 25% of the average signal level at modulation frequencies up to 1.0% of the bit rate.

(c) With data dropouts (no transitions) of 127 bits occurring once every 600 bits.

3. With SNR ≥ 15 dB and 50% transition density, the 720 will maintain synchronization with input signal jitter of ±1.0% at any jitter rate. Refer to Figure 2-4 for typical performance data.

f. Bit Error Performance: For white Gaussian noise with bandwidth greater than five times, but not greater than ten times, the bit rate superimposed on the input bit stream, the bit

error performance of the Model 720 for random data (50% transition density) is as follows:

1. For bit rates up to 2.5 Mbps, the Model 720 performs within 1 dB of the theoretical bit error probabilities for all codes. At higher bit rates, bit error performance degrades to the extent shown in Table 2-2 and is specified only for signal-to-noise ratios above the specified sync threshold.

g. Ideal Bit Error Performance Curves: The curves shown in Figures 2-6 and 2-7 illustrate the best theoretical bit error probabilities versus SNR for each code and mode of operation. The following notes are applicable:

1. The signal-to-noise ratio (SNR) is the ratio of the "steady-state" peak signal to the rms noise measured in the noise reference bandwidth.

2. The "steady-state" peak signal is one half of the peak-to-peak signal voltage that results after all transients have died out. This definition eliminates the dependence of the peak signal level on the data pattern in pre-modulation filtered bit streams.

3. The "noise reference bandwidth" is defined as 0.5 times the bit rate.

4. The curves for square PCM assume the following:

   Input Bit Stream: Random data square PCM with negligible rise time.

   Bit Detector: 100% integrator, sampled at the end of each bit period.

5. The curves for pre-modulation filtered NRZ codes assume the following:

   Pre-Modulation Filter: 6-pole linear phase with 3 dB frequency at .75 bit rate.

   Bit Detector: A 6-pole linear phase filter with 3 dB frequency at .5 bit rate. The output is sampled at the midpoint of each bit period.

6. The curves for pre-modulation filtered BiØ codes are identical to those for NRZ codes, but the following assumptions are made:

   Pre-Modulation Filter: 6-pole linear phase with 3 dB frequency at 1.5 bit rate.

   Bit Detector: A 6-pole bandpass filter with 3 dB frequencies at .5 bit rate and 1.0 bit rate. The output is sampled at the midpoint of the bit period.

7. The bit error performance for the RZ code is exactly 3 dB worse than for the NRZ-L code. For pre-modulation filtered RZ, the pre-modulation filter is a 6-pole linear phase filter with 3 dB frequency at 1.5 bit rate. The bit detector is a 6-pole linear phase filter with 3 dB frequency at bit rate. The output is sampled at the midpoint of the bit period.

8. See Table 2-3 for a numerical tabulation of bit error probability for NRZ-L and DM codes.

h. Bit Error Performance with Other Signal Perturbations: With 50% transition density, bit error performance is degraded less than 1 dB from that specified in (f) above for the following adverse conditions:

   1. Baseline variation specified in 2.2.1 (1).

   2. Amplitude modulation at frequencies up to 1% of bit rate and amplitude up to 25% of the signal amplitude.

2.2.3 Data and Clock Outputs

a. Data for Processing: Serial NRZ-L for all input codes.

b. Bit Rate Clock Outputs: Four separate pulse trains (0°, 90°, 180°, and 270° clocks), synchronous with the serial PCM outputs, are provided. Each clock output is a symmetrical square wave with a maximum departure from symmetry of ± 100 nsec or ± 10% of the bit period, whichever is less.

c. Logic Levels:

1. Logic ONE -- +2.4V DC to +5V DC.

2. Logic ZERO -- 0V DC to +0.4V DC.

d. Drive Capability: Output current limited to 50 mA minimum into a nominal terminating impedance or a short circuit. Output sinks up to 50 mA maximum when in logic ZERO state. The output driver is a low impedance (< 10 Ω) voltage source, designed to drive terminated cables.

e. Rise and Fall Times: 25 nsec maximum.

f. Tape Recorder: Serial BiØ-L and DM (M or S selected by a switch on the Code Converter Card) for all input codes.

1. Level -- 2V peak-to-peak ±20%, centered about ground, into a 50 Ω load. No-load output level is 5V peak-to-peak ±20%. DC offset is less than ±20% of the peak-to-peak voltage.

2. Output Impedance: 70 Ω ±20%.

3. Rise and Fall Times: 25 nsec maximum.

2.2.4 Status Outputs

a. Input Level: "Input high" and "input low" lines provided.

1. Input High -- At logic ONE[1] whenever PCM input level exceeds 20V ±5V peak-to-peak.

2. Input Low -- At logic ONE[1] whenever PCM input level is less than 0.6V ±0.15V peak-to-peak.

b. Deviation Status: "Upper bandedge" and "lower bandedge" lines provided.

1. Upper Bandedge -- At logic ONE[1] whenever incoming
b bit rate exceeds 70% of the tracking range above selected bit rate.

2. Lower Bandedge -- At logic ONE[1] whenever incoming bit rate exceeds 70% of the tracking range below selected bit rate.

c. Power On Status: One line at logic ONE when 720 is energized.

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[1] These logic ONE levels are latched for a minimum of 100 microseconds each time they occur.

d. Remote Status: One line at logic ONE when 720 is in REMOTE mode.

e. Sync Status: One line at logic ONE when 720 is synchronized with PCM input.

f. Operating Program Parameter Readout: The operating program parameters are brought out on parallel lines to rear-panel connectors.

g. Status Signal Output Characteristics:

1. Output Levels --

(a) Logic ONE: +2.4V DC to +5V DC.

(b) Logic ZERO: 0V DC to +0.4V DC.

2. Output Current --

(a) When V_{out} = +0.4V DC, the output will sink 16 mA minimum.

(b) When V_{out} = +2.4V DC, the output will supply 0.4 mA minimum.

3. Rise and Fall Times -- With maximum load at output connector, 25 nsec maximum.

2.2.5 Front-Panel Controls

a. Source: A thumbwheel switch that enables selection of any one of four input sources.

b. Bit Rate: Five thumbwheel switches that provide bit rate selection (to four significant figures) from 1 bps to 5.000 Mbps.

c. Mode Control: Three interlocking pushbutton switches are provided for LOCAL, REMOTE, or OVERRIDE mode of operation.

1. LOCAL -- All functions are directly controlled by the front-panel programming switches.

2. REMOTE -- All functions are controlled by static stores programmable by a computer or similar device.

3. OVERRIDE -- Permits operator to selectively modify internally-stored program by front-panel switches. When in OVERRIDE, computer entry is locked out.

d. Input Code: Nine interlocking pushbutton switches that provide selection of NRZ-L, NRZ-M, NRZ-S, RZ, BiØ-L, BiØ-M, BiØ-S, DM-M and DM-S.

e. Data Polarity: Two interlocking pushbutton switches that provide selection of normal or inverted input polarity.

f. Detector: Two interlocking pushbutton switches that provide bit decision feedback when pre-modulation filtered data is being received.

g. Loop Width: Three interlocking pushbutton switches that provide selection of 1%, 0.3%, or 1.0% loop widths. Respective tracking ranges of 1%, 3% and 10% are automatically selected with these loop widths.

h. Enter: Pushbutton switches provided for loading static stores by front-panel controls when in OVERRIDE mode, for each of these selective functions: input code, input source, bit rate, polarity, loop width, and filter detection.

i. Power: Pushbutton switch controls application of primary power to the unit.

2.2.6 Front-Panel Displays

a. Functional Status: The operating parameters of the 720 are displayed by light-emitting diode indicators under the appropriate function titles. Bit rate and input source are displayed by numeric indicators.

b. Input Meter: Indicates input signal level.

c. Deviation Meter: Indicates deviation of the input bit rate from the selected bit rate. (The white area of the meter scale denotes the selected tracking range.)

d. Sync: Illuminates to indicate that the 720 is phase locked with the input signal.

e. Signal Loss: Illuminates to indicate that the input signal level has dropped below the minimum acceptable voltage or when there have been 128 consecutive bit periods without a transition in NRZ and RZ codes.

f. Power: Illuminates to indicate that primary power has been applied to the unit.

2.2.7 Test

Test Points: Short-circuit-proof front-panel pin jacks are provided for INPUT, NRZ-L OUT, 0° CLOCK, and GROUND.

2.2.8 Remote Programming

a. Programmable Functions: Source, bit rate, input code, data polarity, loop width, and PCM detector.

b. Instruction Format: A 16-bit word containing the following fields:

1. Module Address -- Four-bit field, selectable by means of internal jumper wire, allows addressing a particular unit and programming by remote control.

2. Group Address -- Four-bit field, specifies the group of operating parameters being addressed.

3. Instruction -- Eight-bit field contains the required function parameter to be entered into the static stores.

c. Instruction Request: One line, at the logic ONE level when an instruction can be entered into the static stores; at the logic ZERO level to inhibit instruction entry.

d. Instruction Transfer: One line (normally at the logic ZERO level), which causes entry of an instruction when it goes to a logic ONE level, subject to the Instruction Request status.

2.2.9 Remote Control Logic Levels

a. Input Levels:

1. Logic ONE -- +2.4V DC to +5V DC.

2. Logic ZERO -- 0V DC to +0.4V DC.

b. Input Current: 1.60 mA maximum, out; V_{in} = 0V. .04 mA maximum, in; V_{in} = +5V.

c. Noise Immunity: The input will recognize 0V to +0.8V as a logic ZERO and +2.0V to +5V as a logic ONE.

d. Output Levels: Same as "Status Signal Output Characteristics," paragraph 2.2.4 (g).

e. Output Current: Same as "Status Signal Output Characteristics," paragraph 2.2.4 (g).

f. Rise and Fall Times: Same as "Status Signal Output Characteristics," paragraph 2.2.4 (g).

2.2.10 Power Requirement

a. Voltage:

1. 105V to 132V rms, 47 Hz to 65 Hz.

2. 105V to 132V rms, 360 Hz to 440 Hz.

3. 207V to 253V rms, 47 Hz to 65 Hz.

b. Power: 120 watts.

2.3 MECHANICAL SPECIFICATIONS

a. Panel Size: 5-1/4 inches high by 19 inches wide (13.3 by 48.3 cm).

b. Overall Depth: 21-1/2 inches (54.6 cm), excluding rear-mounted connectors and projections from the front panel.

c. Weight: Net, 35 pounds (15.9 kg). Shipping, 60 pounds (27.2 kg).

d. Panel Finish: Front-panel color is semi-gloss gray, No. 26492 per FED-STD-595. Lettering is black. Other panel and lettering paints are available.

e. Mounting: Slides and hardware for installation in an EIA-type rack can be provided.

f. Rear-Panel Input/Output Connectors: As shown in Figure 3-1, twelve BNC connectors and three Amphenol-type 220-1N052 with a locking device are used. Mating connectors (except for BNC's) are supplied with each unit. A power connector and mating power cord are also supplied.

2.4 ENVIRONMENTAL SPECIFICATIONS

a. Temperature: Operating, 0°C to +50°C. Non-operating, -55°C to +71°C.

b. Altitude: Operating, sea level to 10,000 feet.

c. Humidity: Operating, 0 to 95% without condensation.

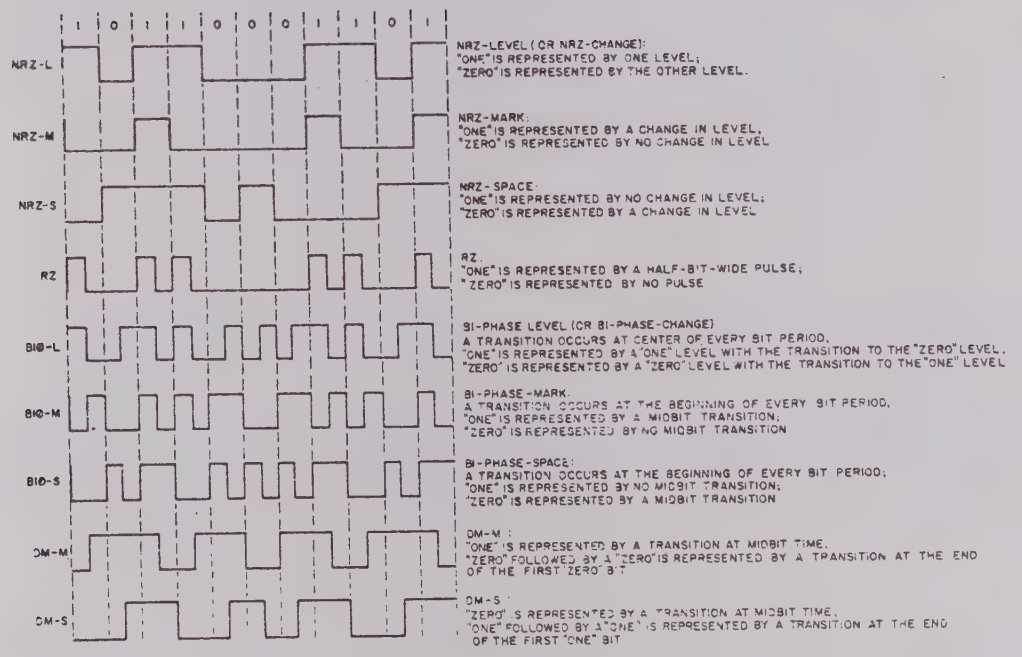
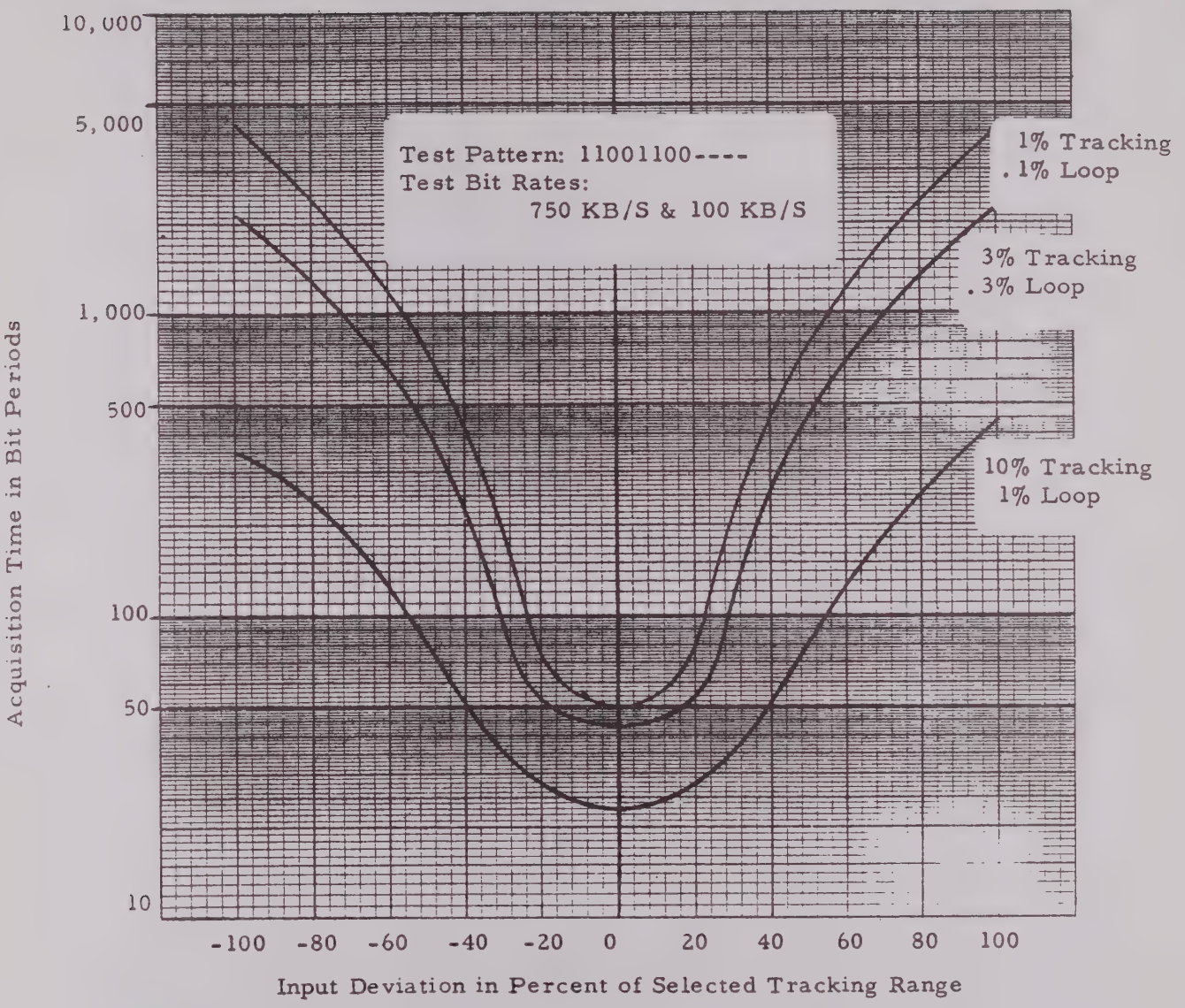


Figure 2-1. PCM Input Codes



NOTES:

1. Typical acquisition performance for Model 720 for NRZ and Bi-Phase Codes at 15 dB SNR.
2. Acquisition time approximately 100% longer for RZ code.

Figure 2-2. Acquisition Time Versus Deviation of Input Bit Rate From Selected Bit Rate

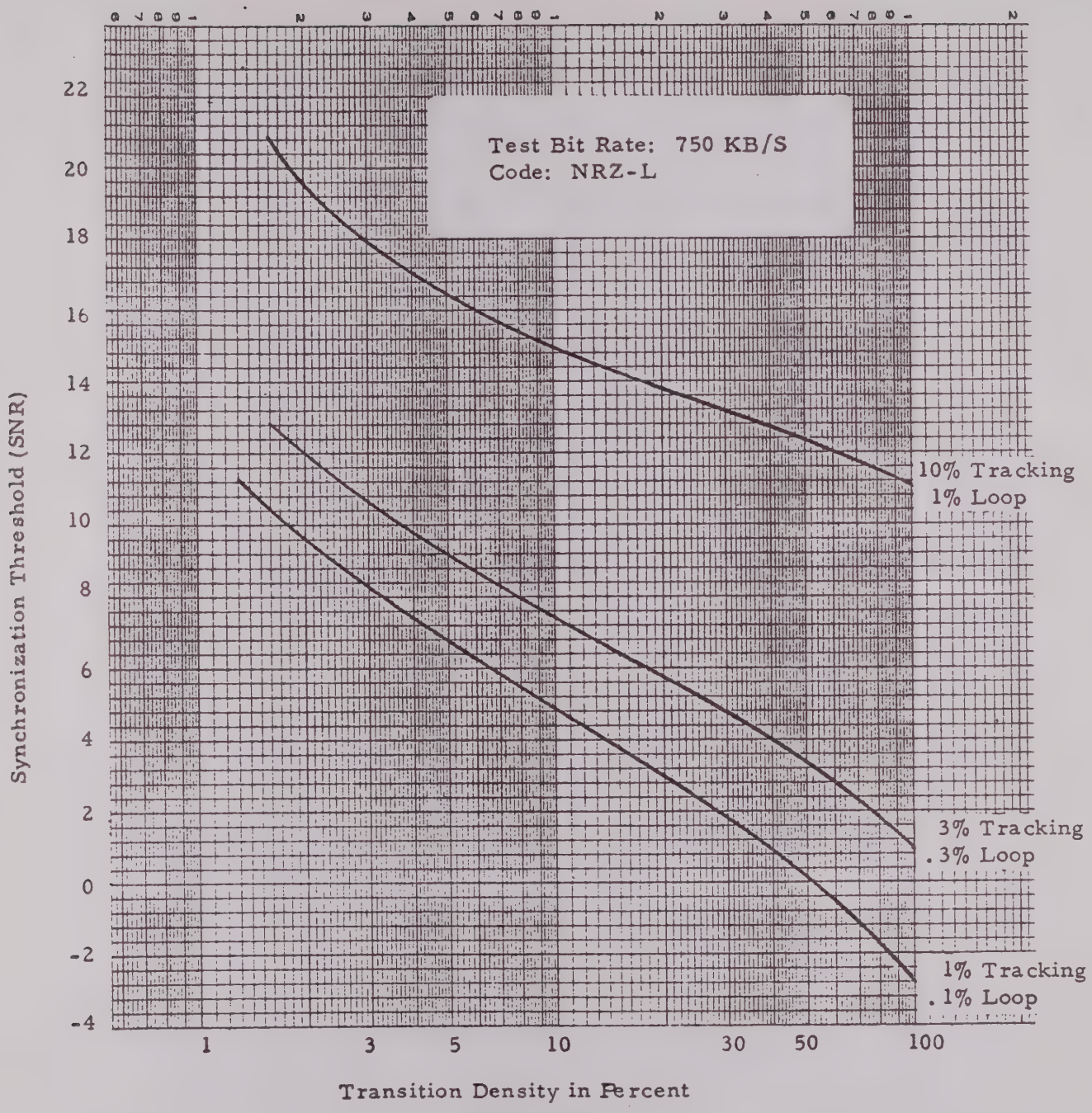
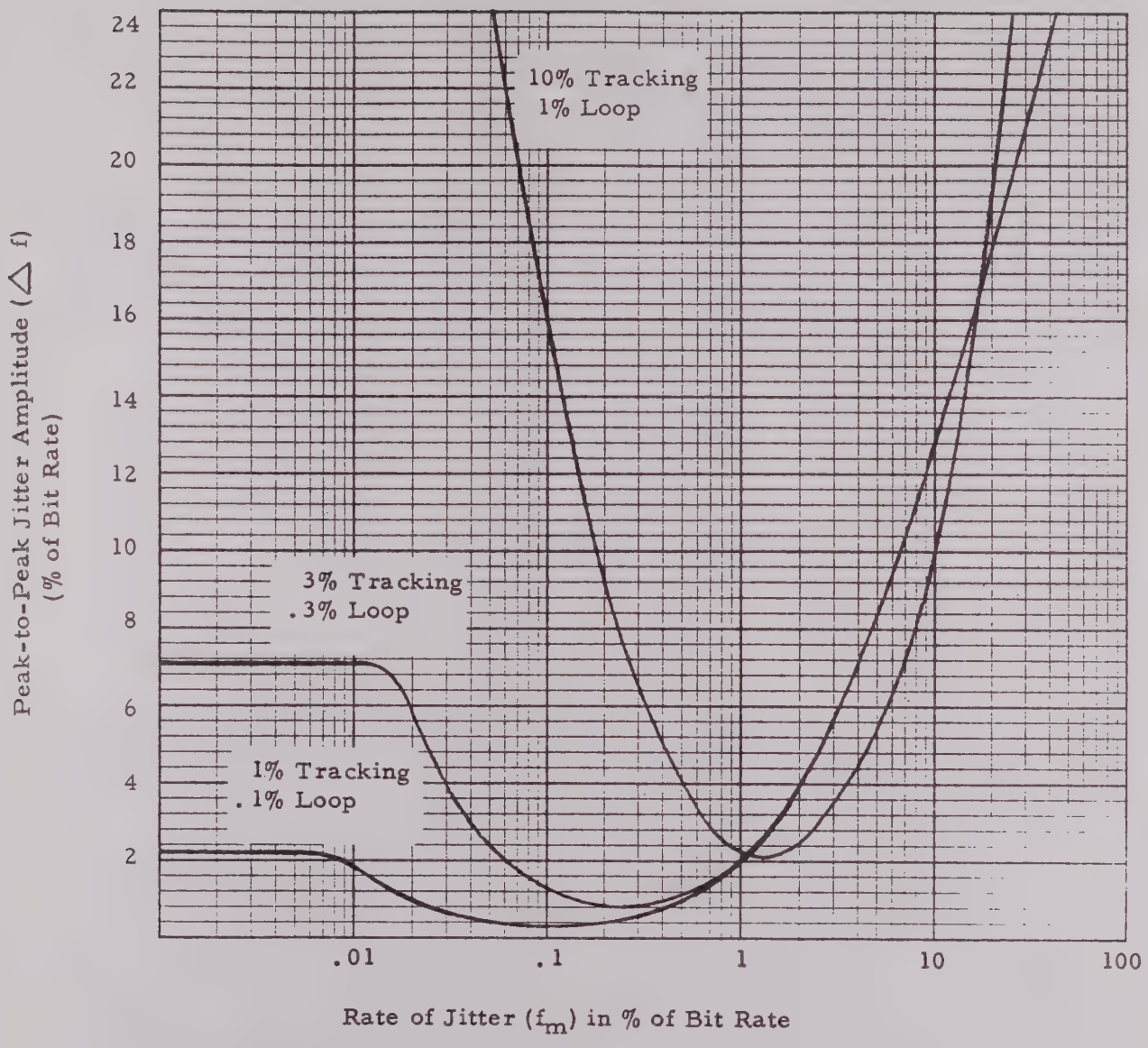


Figure 2-3. Synchronization Threshold Versus Transition Density (Typical Model 720 Performance)



Notes:

1. The area under the curve is the valid operating area for maintenance of synchronization.
2. Actual data measured on the 720 under the following conditions: SNR = 15 db; Code: NRZ-L; Bit Rate: 100 K BPS; Pattern: 1110111110101100
3. The above performance is typical for the 720 for all codes and bit rates.

Figure 2-4. Maximum Peak-to-Peak Jitter (Sine Wave) Versus Rate of Jitter for Maintenance of Synchronization

TEST SETUP

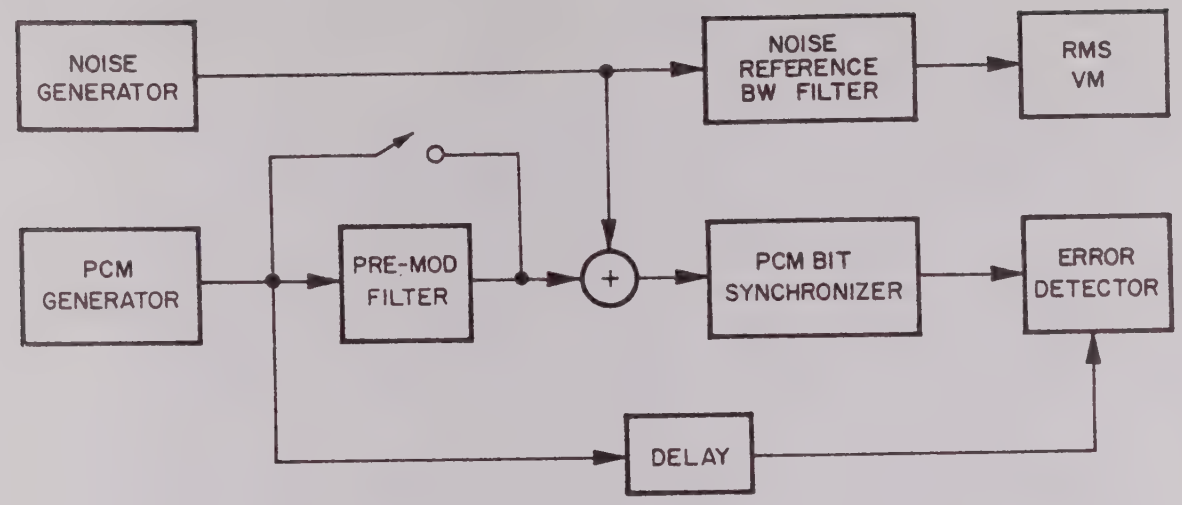


Figure 2-5. Test Setup for Figures 2-6 and 2-7

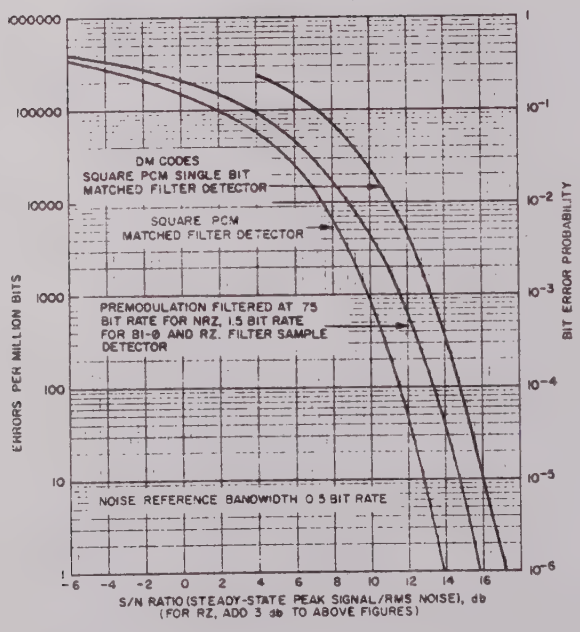


Figure 2-6. Ideal Bit Error Performance for NRZL, BiØL, RZ and DM

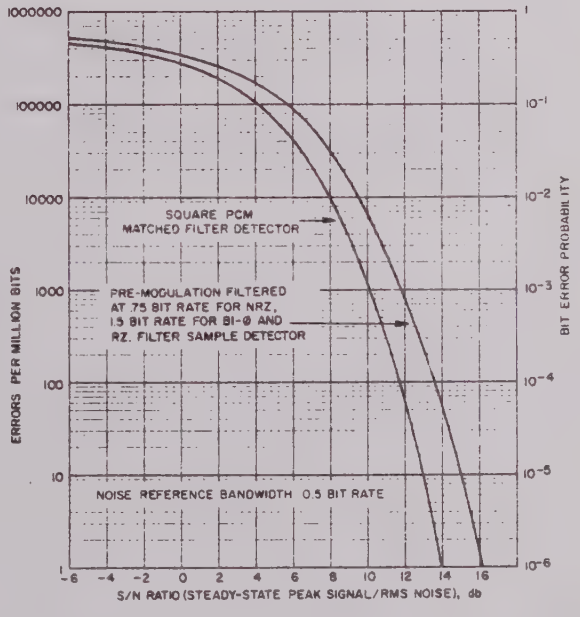


Figure 2-7. Ideal Bit Error Performance for NRZM, NRZS, BiØM, and BiØS

Table 2-1. Sync Threshold Limit for All Input Codes at Different Bit Rates

BIT RATE RANGE	CODE			
	NRZ	RZ	Biø	DM
1 bps to 2.5 Mbps	3 dB	3 dB	3 dB	6 dB
2.5 Mbps to 4.0 Mbps	3 dB	3 dB	6 dB	9 dB
4.0 Mbps to 5.0 Mbps	3 dB	3 dB	6 dB	12 dB

Refer to Figure 2-3 for typical synchronization threshold performance.

NOTE

To verify the level of synchronization threshold, instrumentation errors must be accounted for. An additional margin of error of 0.5 dB is permissible.

Table 2-2. Bit Error Performance

Bit Rate Range	CODE							
	NRZ		RZ		Biø		DM	
	Sync Threshold	Performance Limit from Theoretical	Sync Threshold	Performance Limit from Theoretical	Sync Threshold	Performance Limit from Theoretical	Sync Threshold	Performance Limit from Theoretical
1 bps to 2.5 Mbps	3 dB	1 dB	3 dB	1 dB	3 dB	1 dB	6 dB	1 dB
2.5 Mbps to 4.0 Mbps	3 dB	2 dB	3 dB	3 dB	6 dB	2 dB	9 dB	3 dB
4.0 Mbps to 5.0 Mbps	3 dB	2 dB	3 dB	4 dB	6 dB	3 dB	12 dB	3 dB

NOTE

To verify the level of performance, instrumentation errors must be accounted for. An additional margin of error of 0.5 dB is permissible.

Table 2-3. Bit Error Probability for NRZ-L and DM Codes

SNR (1) in dB	Theoretical Bit Error (2) Probability	
	NRZ-L	DM
0	1.58×10^{-1}	4.80×10^{-1}
3	7.86×10^{-2}	3.17×10^{-1}
6	2.31×10^{-2}	1.57×10^{-1}
9	2.34×10^{-3}	4.62×10^{-2}
10	8.06×10^{-4}	2.55×10^{-2}
11	1.93×10^{-4}	1.20×10^{-2}
12	3.53×10^{-5}	4.68×10^{-3}
13	4.05×10^{-6}	1.61×10^{-3}
14	2.77×10^{-7}	3.86×10^{-4}
15	9.86×10^{-9}	7.07×10^{-5}
16		8.10×10^{-6}
17		5.55×10^{-7}
18		1.97×10^{-8}

Notes:

1. SNR defined as the ratio peak signal to rms noise referenced to a noise bandwidth of 0.5 x bit rate.

2. Single bit period, matched filter detection.

Table 2-4. EMR 720 Bit Synchronizer, Model Number Identification

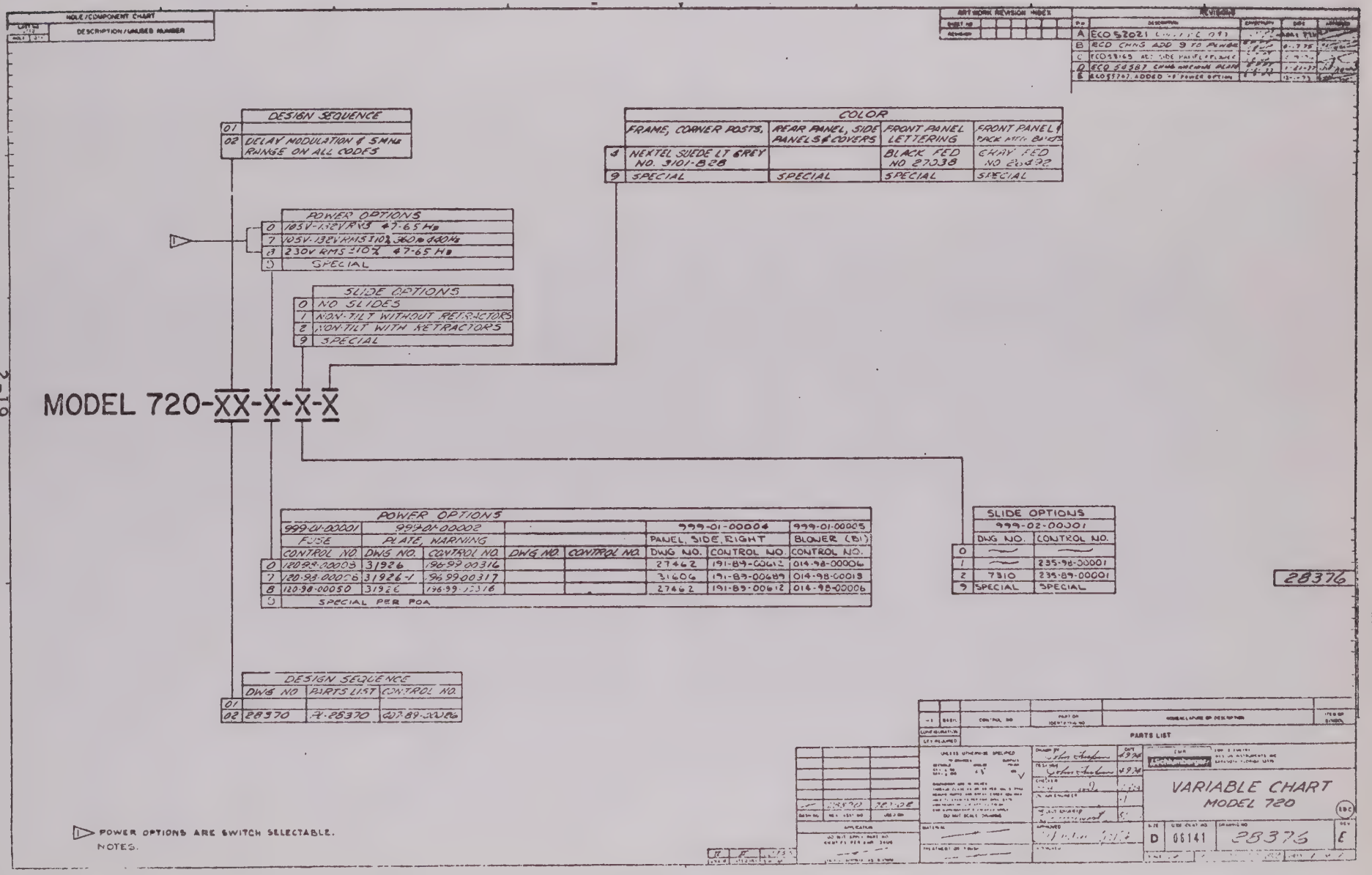


Table 2-5. PCM Bit Synchronizer Definitions

TERM	DEFINITION
Acquisition	The process of the bit synchronizer clock achieving frequency and phase lock with the incoming bit stream.
Baseline	The center line of the signal; the voltage level midway between the peaks.
Bi-Phase Ambiguity	The ambiguous nature of BiØ-L code where it is impossible to determine whether a string of bits of the same logic level is a string of logic ONE's or logic ZERO's, since the signal is a continuous square wave at the bit rate.
Bit Rate Deviation	The difference between the incoming bit rate and the selected bit rate, specified in terms of percent of the selected bit rate.
Bit Slippage	The increase or decrease in the clock frequency by one or more bits with respect to the input signal.
Capture Range	The maximum bit rate deviation for which the bit synchronizer will acquire synchronization with the incoming bit stream.
Clock Error	A phase error in excess of $\pm 90°$ between the output clock and the clock to which the input signal is referenced. This phase error produces one clock error each bit period.
Jitter	Frequency modulations of the input bit rate. The jitter amplitude (Δf) is the maximum percentage of bit rate by which the instantaneous bit rate deviates from the nominal bit rate. The "rate of jitter" (f_m) is the rate (in percentage of bit rate) at which the bit rate is being modulated.
Loop Bandwidth	The natural frequency (ω_n) of the phase-lock loop. The natural frequency is the frequency at which the loop would be resonant if the damping factor were zero.
Noise Reference Bandwidth	The bandwidth to which the rms noise level is referred when determining a SNR.
Premodulation Filter	The filter through which the PCM stream is passed prior to modulating a carrier and being transmitted.
Random Data	Data generated by random noise pulse-code modulating the bit rate. It is assumed that random data has a 50% transition density.

Table 2-5 (Cont'd.). PCM Bit Synchronizer Definitions

TERM	DEFINITION
Signal Loss	The absence of transitions for 128 consecutive bit periods, or an input voltage level less than the specified minimum input peak-to-peak voltage (including noise).
Signal-to-Noise Ratio (SNR)	The ratio of steady-state peak signal to rms noise in the noise reference bandwidth.
Steady-State Peak Signal	One half of the peak-to-peak signal voltage that results after all transients have died out.
Synchronization	The bit synchronizer is defined as being "synchronized" to the input bit stream when bit slippage is less than one bit per million.
Synchronization Acquisition Time	The length of time, in bit periods, required for the bit synchronizer clocks to become synchronized with the incoming bit stream.
Synchronization Threshold	The minimum SNR at which synchronization is maintained.
Tracking Range	The maximum bit rate deviation that the bit synchronizer will track and remain synchronized with the incoming bit stream.
Transition	A change in voltage level which crosses the threshold between the two logic states, regardless of whether or not the change in level represents a change in the data.
Transition Density	The average number of transitions expressed as a percentage of the maximum possible number of transitions.

OPERATION

SECTION 3

INSTALLATION AND OPERATION

3.1 INSTALLATION

The EMR 720 is shipped completely assembled and ready for mounting. The unit should be inspected immediately on its arrival and notice given to EMR-Telemetry of any claim that the product does not conform with the terms of the order.

The 720 is designed for mounting in a standard 19-inch EIA equipment rack or portable instrument case. Physical dimensions of the unit are listed in Section 2. Installation is dependent upon the type of mounting slides provided with the unit. If no slides are purchased, the installation is performed in accordance with the customer requirements. When mounting slides are purchased, hardware is also supplied for a direct installation in the mounting equipment.

The general method for unit installation when slides are provided is as follows:

a. Remove the unit from the shipping carton.

b. Remove the outside brackets of each slide.

c. Mount these brackets to the internal frame of the mounting equipment.

d. Insert the unit into the slides and push the unit into the slides until the unit is locked in position.

Captive screws are provided on each side of the front panel to secure the unit in the mounting equipment. The unit may be extended from the rack for checkout, adjustment, or troubleshooting by pulling straight out; stop latches on the slide hold the unit at the maximum extension.

After installing the unit, the external electrical connections are terminated at rear-panel connectors. A rear-panel view is shown in Figure 3-1. A list of the connectors and the type of connections to be terminated is contained in Table 3-1. Tables 3-2 through 3-4 provide signal identification data for 52-pin connectors A4J1 through A4J3. Also illustrated on Figure 3-1 is toggle switch A4S1 which enables locking the 720 VCO to an external clock rather than the incoming PCM signal.

3.2 BIT SYNCHRONIZER PROGRAMMING

The programming mode (LOCAL or REMOTE) of the 720 is selected at the unit's front panel. In the LOCAL mode, all programmable functions are controlled directly by front-panel switches. In the REMOTE mode, all programmable

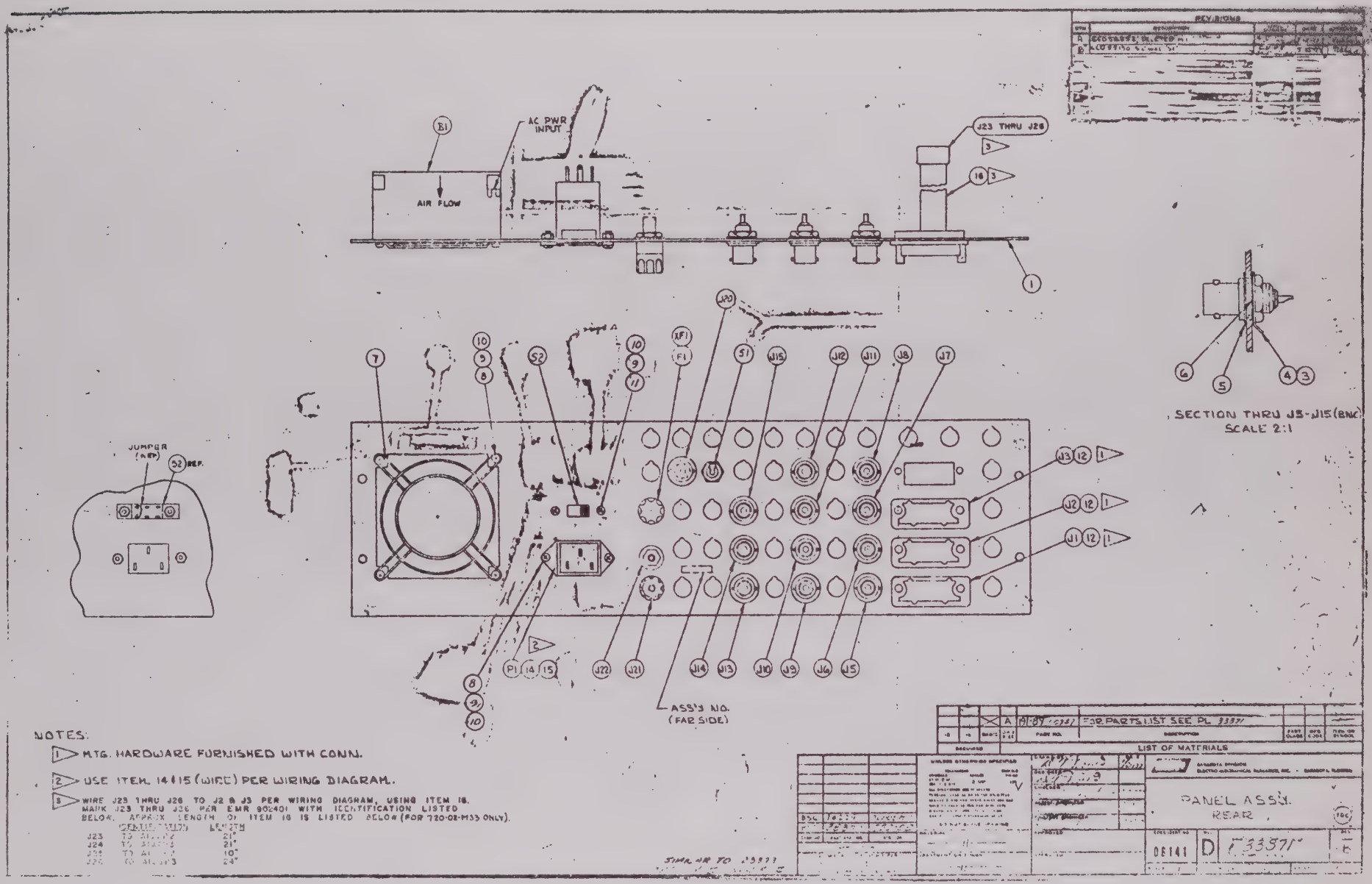


Figure 3-1. Model 720 Rear-Panel Connectors

Table 3-1. Model 720 Rear-Panel Connectors

CONNECTOR REFERENCE DESIG.	CONNECTOR TYPE	FUNCTION
A4P1	EMR 5351	Power
A4J1	Amphenol 220-1N052	Remote Instruction
A4J2	Amphenol 220-1N052	Status Output 1
A4J3	Amphenol 220-1N052	Status Output 2
A4J4	- - -	- - -
A4J5	BNC	Source 1
A4J6	BNC	Source 2
A4J7	BNC	Source 3
A4J8	BNC	Source 4
A4J9	BNC	0° Clock
A4J10	BNC	90° Clock
A4J11	BNC	180° Clock
A4J12	BNC	270° Clock
A4J13	BNC	NRZ-L Output
A4J14	BNC	Biø-L Output
A4J15	BNC	DM Output
A4J16	- - -	- - -
A4J17	- - -	- - -
A4J18	- - -	- - -
A4J19	- - -	- - -
A4J20	BNC	External Clock Input
A4J21	Superior DF-30BC	Signal Ground
A4J22	Superior GP-30NC	Chassis Ground

Table 3-2. Remote Instruction Connector (A4J1) Signal Identification

PIN	SIGNAL
A4J1A2	Remote Instruction, Bit 1 (LSB)
A4J1B1	Ground
A4J1A4	Remote Instruction, Bit 2
A4J1B3	Ground
A4J1A6	Remote Instruction, Bit 3
A4J1B5	Ground
A4J1A8	Remote Instruction, Bit 4
A4J1B7	Ground
A4J1A10	Remote Instruction, Bit 5
A4J1B9	Ground
A4J1A12	Remote Instruction, Bit 6
A4J1B11	Ground
A4J1D13	Remote Instruction, Bit 7
A4J1B13	Ground
A4J1C2	Remote Instruction, Bit 8 (MSB)
A4J1D1	Ground
A4J1C4	Remote Group Address, Bit 9
A4J1D3	Ground
A4J1C6	Remote Group Address, Bit 10
A4J1D5	Ground
A4J1C8	Remote Group Address, Bit 11
A4J1D7	Ground

PIN	SIGNAL
A4J1C10	Not Used
A4J1D9	Ground
A4J1C12	Module Address, Bit 13
A4J1D11	Ground
A4J1E2	Module Address, Bit 14
A4J1F1	Ground
A4J1E4	Module Address, Bit 15
A4J1F3	Ground
A4J1E6	Module Address, Bit 16
A4J1F5	Ground
A4J1E8	Instruction Transfer
A4J1F7	Ground
A4J1E10	Instruction Request
A4J1F9	Ground
A4J1E12	Remote
A4J1F11	Ground
A4J1H13	Power On
A4J1F13	Ground
A4J1G2	Input Level Low
A4J1H1	Ground
A4J1G4	Input Level High
A4J1H3	Ground
A4J1G6	Upper Bandedge
A4J1H5	Ground
A4J1G8	Lower Bandedge
A4J1H7	Ground
A4J1G10	Sync
A4J1H9	Ground
A4J1G12	No Connection
A4J1H11	Ground

Table 3-3. Status 1 Connector (A4J2) Signal Identification

PIN	SIGNAL
A4J2A2	BR 1-1
A4J2B1	Ground
A4J2A4	BR 1-2
A4J2B3	Ground
A4J2A6	BR 1-4
A4J2B5	Ground
A4J2A8	BR 1-8
A4J2B7	Ground
A4J2A10	BR 2-1
A4J2B9	Ground
A4J2A12	BR 2-2
A4J2B11	Ground
A4J2B13	Ground
A4J2C2	BR 2-4
A4J2D1	Ground
A4J2C4	BR 2-8
A2J2D3	Ground
A4J2C6	BR 3-1
A4J2D5	Ground
A4J2C8	BR 3-2
A4J2D7	Ground
A4J2C10	BR 3-4
A4J2D9	Ground
A4J2C12	BR 3-8
A4J2D11	Ground
A4J2D13	Ground
A4J2E2	BR 4-1
A4J2F1	Ground

PIN	SIGNAL
A4J2E4	BR 4-2
A4J2F3	Ground
A4J2E6	BR 4-4
A4J2F5	Ground
A4J2E8	BR 4-8
A4J2F7	Ground
A4J2E10	No Connection
A4J2F9	Ground
A4J2E12	No Connection
A4J2F11	Ground
A4J2F13	Ground
A4J2G2	Input Level Low
A4J2H1	Ground
A4J2G4	Input Level High
A4J2H3	Ground
A4J2G6	Upper Bandedge
A4J2H5	Ground
A4J2G8	Lower Bandedge
A4J2H7	Ground
A4J2G10	Sync
A4J2H9	Ground
A4J2G12	No Connection
A4J2H11	Ground
A4J2H13	Ground

Table 3-4. Status 2 Connector (A4J3) Signal Identification

PIN	SIGNAL	PIN	SIGNAL
A4J3A2	NRZL Code	A4J3E2	DM-M Code
A4J2B1	Ground	A4J3F1	Ground
A4J3A4	Square PCM	A4J3E4	1% Tracking *
A4J3B3	Ground	A4J3F3	Ground
A4J3A6	NRZM Code	A4J3E6	DM-S Code
A4J3B5	Ground	A4J3F5	Ground
A4J3A8	NRZS Code	A4J3E8	No Connection
A4J3B7	Ground	A4J3F7	Ground
A4J3A10	BiØL Code	A4J3E10	2^0
A4J3B9	Ground	A4J3F9	Ground
A4J3A12	BiØM Code	A4J3E12	2^1
A4J3B11	Ground	A4J3F11	Ground
A4J3B13	Ground	A4J3F13	Ground
A4J3C2	BiØS Code	A4J3G2	2^2
A4J3D1	Ground	A4J3H1	Ground
A4J3C4	RZ Code	A4J3G4	Polarity Normal
A4J3D3	Ground	A4J3H3	Ground
A4J3C6	10% Tracking *	A4J3G6	No Connection
A4J3D5	Ground	A4J3H5	Ground
A4J3C8	Bit Rate Mult. 1	A4J3G8	No Connection
A4J3D7	Ground	A4J3H7	Ground
A4J3C10	Bit Rate Mult. 2	A4J3G10	No Connection
A4J3D9	Ground	A4J3H9	Ground
A4J3C12	Bit Rate Mult. 4	A4J3G12	No Connection
A4J3D11	Ground	A4J3H11	Ground
A4J3D13	Ground	A4J3H13	Ground

** (A4J3E10, A4J3F9, A4J3E12, A4J3F11, A4J3F13, A4J3G2, A4J3H1)

* Logic ONE on either line indicates corresponding tracking has been selected. Logic ZERO on both lines indicates 3% tracking has been selected.

** 3-bit binary code (2^0, 2^1, 2^2) indicating input source selection.

functions are computer-controlled and the program parameters are stored in the instruction storage registers. In this manner, switching from one programming mode to the other does not destroy the program setup for the previous mode. When under REMOTE control, any program parameter stored in the instruction storage registers may be modified at the front panel by depressing the OVERRIDE pushbutton, changing the program parameter at the corresponding front-panel control, and then depressing the corresponding ENTER button. REMOTE programming is inhibited during OVERRIDE.

Under REMOTE control, 720 programming is accomplished via a control interface consisting of 16 data lines, one instruction request line, and one instruction transfer line. As shown in the programming format (Table 3-5), five 16-bit parallel words are required to load the instruction storage registers. Each parallel data word contains the following information: Four bits (13 through 16) are used for the module (unit) address (customer assigned), four bits (9 through 12) are used for the group address which determines the internal functions being addressed, and eight bits (1 through 8) contain the actual instructions. The instruction request is a 720 output (to the remote programming source) that indicates whether or not the unit is ready to accept programming instructions. The instruction transfer line strobe is an output (from the remote programming source) which accompanies each 16-bit parallel word and enables instruction entry into the 720 instruction storage registers, subject to the status of the instruction request line. Timing for the REMOTE programming of the 720 is shown in Figure 3-2.

3.3 OPERATION

3.3.1 Front-Panel Controls, Indicators, and Monitor Jacks

The front-panel components are illustrated in Figure 3-3. Functional descriptions of these components are furnished in Table 3-6.

3.3.2 Selection of Internal or External Clock

Selection of the internal or external clock is controlled at rear-panel toggle switch A4S1 (INT/EXT). The external clock is received at rear-panel BNC connector A4J20. The external clock input is provided to allow phase-locking the 720 internal clocks with an external clock. When the external clock input is used, this signal is routed to the phase detector [which otherwise receives the timing signals ($SYNC^2$) generated in the input filter from the incoming bit stream]. The phase-lock-loop then locks onto the external clock. If the input code selected is DM, the external clock signal must be at twice the bit rate. For all other codes, the external clock must be at bit rate.

3.3.3 Operation in the LOCAL Mode

To program the bit synchronizer at the front panel, proceed as follows:

a. Make input/output connections at bit synchronizer rear panel as required (refer to Table 3-1 for signal identification data).

b. Select internal (INT) or external (EXT) clock at bit synchronizer rear panel. For normal bit sync operation (synchronizing to an input PCM stream), always use the INT clock position.

c. Select manual mode of operation by depressing LOCAL mode pushbutton.

d. Apply power to bit synchronizer by energizing POWER pushbutton.

e. Select bit synchronizer operating parameters at appropriate thumbwheel/pushbutton switches.

3.3.4 Operation in the REMOTE and OVERRIDE Modes

To program the bit synchronizer (1) from a remote source (a computer or similar device) and (2) to OVERRIDE this program, proceed as follows:

a. Make input/output connections at bit synchronizer rear panel as required (refer to Table 3-1 for signal identification data).

b. Select internal (INT) or external (EXT) clock at bit synchronizer rear panel. For normal bit sync operation (synchronizing to an input PCM stream), always use the INT clock position.

c. Place bit synchronizer in either LOCAL or OVERRIDE.

d. Apply power to bit synchronizer by energizing POWER pushbutton.

e. At remote source, prepare programming format as described in paragraph 3.2.

f. Depress the REMOTE pushbutton and verify program entry by observing the contents of all static stores at the front-panel functional status displays.

g. To modify any operating parameters, proceed as follows:

1. Depress OVERRIDE pushbutton.

2. Change operating parameter(s) and depress corresponding ENTER pushbutton(s).

3. Depress REMOTE pushbutton.

Table 3-5. Model 720 Programming Format

720 PROGRAMMING

MODULE ADDRESS				GROUP ADDRESS				INSTRUCTION								
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
*				0	0	0	1	MSD 8	MSD 4	MSD 2	MSD 1	2ND SD 8	2ND SD 4	2ND SD 2	2ND SD 1	BIT RATE 1ST 2 DIGITS (BCD)
*				0	0	1	0	3RD SD 8	3RD SD 4	3RD SD 2	3RD SD 1	LSD 8	LSD 4	LSD 2	LSD 1	BIT RATE LAST 2 DIGITS (BCD)
*				0	0	1	1	NOT USED X	NOT USED X	NOT USED X	NOT USED X	NOT USED X	4	2	1	BIT RATE MULTIPLIER (POWERS OF 10)
*	-			0	1	0	0	DM-S	DET	SOURCE 4	SOURCE 2	SOURCE 1	POL.	TRACKING		OTHER OPERATING PARAMETERS
*				0	1	0	1	DM-M	NRZL	NRZM	NRZS	RZ	BiØ-L	BiØ-M	BiØ-S	INPUT CODE

* THE 720 MODULE ADDRESS IS VARIABLE AND IS CONTROLLED BY JUMPER CONNECTIONS ON BIT RATE STORE CARD 7.

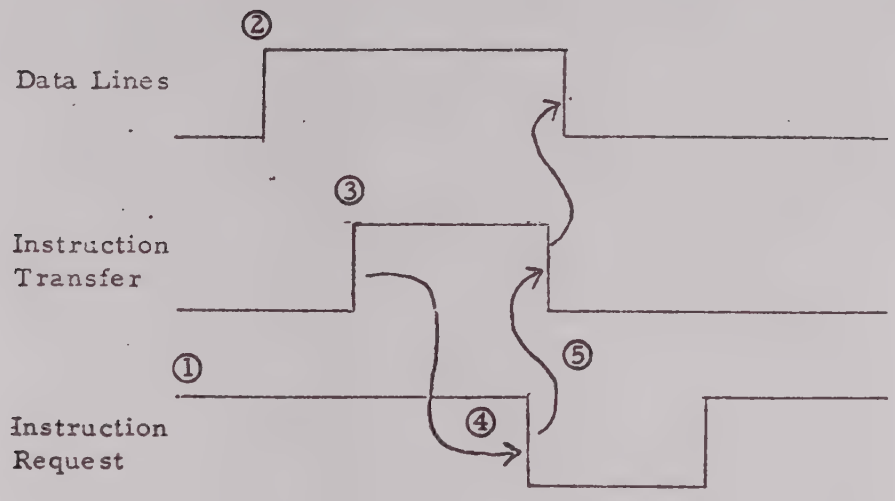
BIT RATE SOURCE INPUT CODE } 1 - ACTIVATES

POL 1 - NORMAL, 0 - INVERT

DET 1 - I/D, 0 - F/S

TRACKING BIT 2	1	
0	1	1%
0	0	3%
1	0	10%

B.R. MULT BIT 4	2	1	
0	0	0	1 B
0	0	1	10 B
0	1	0	100 B
0	1	1	1 KB
1	0	0	10 KB
1	0	1	100 KB
1	1	0	1 MB



Typical Programming Sequence:

① Instruction Request is normally HIGH, indicating the 720 is ready for an instruction.

② Data lines contain correct programming information.

③ Instruction Transfer leading edge loads data into 720 stores. (Data must be stable at least 100 nsec before Instruction Transfer is raised, and must remain at least 100 nsec after Instruction Transfer is raised.)

④ The 720 drops Instruction Request 200 nsec after Instruction Transfer is raised, indicating the data has been loaded.

⑤ The computer can use the negative-going edge of Instruction Request to reset the Data and Instruction Transfer lines.

Figure 3-2. Model 720 Remote Programming Commands

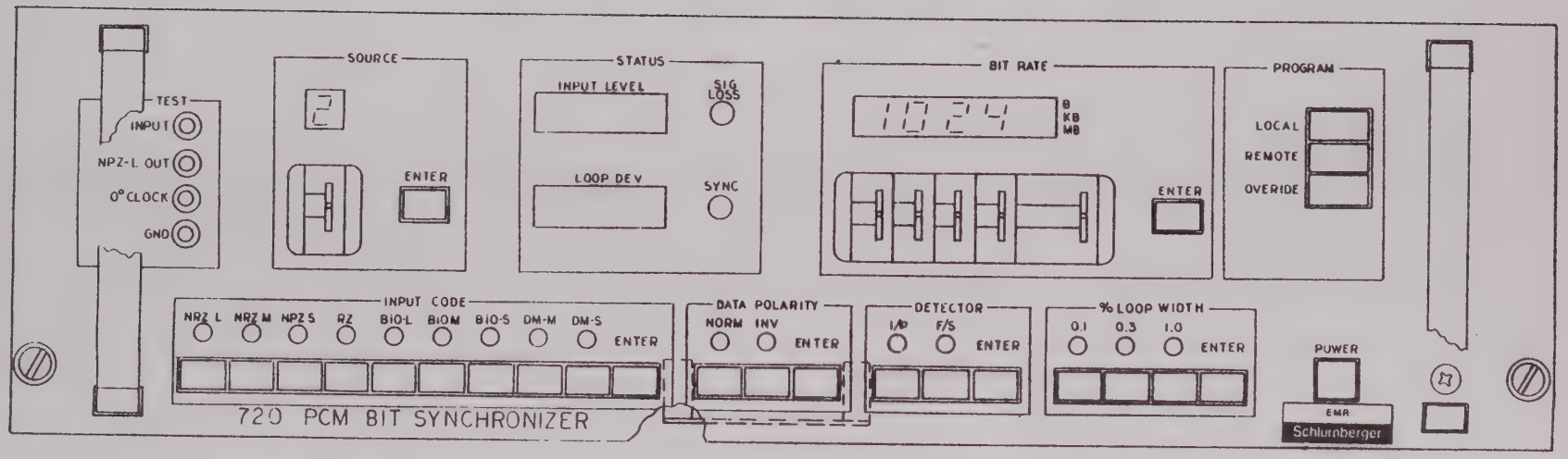


Figure 3-3. Front-Panel Controls and Indicators

Table 3-6. Function of Front-Panel Controls, Indicators, and Monitor Jacks (Ref. Figure 3-3)

NAME	DESIGNATION	FUNCTION
TEST Jacks: INPUT NRZ-L OUT 0° CLOCK GRD	A2TP1 through A2TP4	Short-circuit-proof front-panel pin jacks are provided for monitoring: INPUT, NRZ-L OUT, 0° CLOCK, and GRD.
SOURCE Indicator (Light Emitting Diode)	A2U1	Numeric display of source selected.
SOURCE Thumbwheel	A2S9	A thumbwheel switch that enables selection of any one of four input sources.
ENTER Pushbutton	A2S2	Pushbutton switch provided to load source selection into static stores.
INPUT LEVEL Meter	A2M1	Indicates input signal level in volts peak-to-peak.
LOOP DEV Meter	A2M2	Indicates deviation of input bit rate from selected bit rate. The center of the meter indicates zero deviation, a white area extends to each bandedge. From bandedge to the limits of meter movement, the scale is red.
SIG LOSS Indicator	A2DS1	Lights to indicate that the input signal level has dropped below the minimum acceptable level (0.5V peak-to-peak) or when there have been 128 consecutive bit periods without a transition.
SYNC Indicator	A2DS2	Lights to indicate that the 720 is phase locked with incoming signal.
BIT RATE Indicators (Light Emitting Diodes)	A2U4 through A2U8	Five numeric displays that indicate the bit rate selected. The bit rate is displayed in bits (B), kilobits (KB), and megabits (MB) over the range of 1 bps to 5 Mbps.

Table 3-6 (Cont'd.). Function of Front-Panel Controls, Indicators, and Monitor Jacks (Ref. Figure 3-3)

NAME	DESIGNATION	SIGNAL
BIT RATE Thumbwheels	A2S3 through A2S7	Four thumbwheel switches provide bit rate selection (to four significant figures). The fifth switch provides for decimal and multiplier insertion.
ENTER Pushbutton	A2S8	Pushbutton switch provided to enter bit rate selection into static stores.
Mode Interlocking Pushbuttons	A2S1	Three-stage interlocking pushbutton switch is provided for LOCAL, REMOTE, or OVERRIDE mode of operation. LOCAL: All functions are directly controlled by the front-panel programming switches. REMOTE: All functions are controlled by static stores programmable by a computer or similar device. OVERRIDE: Permits operator to selectively modify internally-stored program by front-panel switches. When in OVERRIDE, computer entry is locked out.
POWER Pushbutton	A3S1	Controls application of primary power to unit.
% LOOP WIDTH Pushbutton Switch Assembly	A1S4	This switch assembly contains three interlocking pushbutton switches that provide selection of 0.1%, 0.3% or 1.0% of selected bit rate loop widths. Respective tracking ranges of 1%, 3%, and 10% are automatically selected with these loop widths. A momentary contact ENTER pushbutton is provided to enter the selected tracking range into static stores.
% LOOP WIDTH -- 0.1%, 0.3%, 1.0% Indicators	A2CR13 through A2CR15 (LED's)	Displays the loop width selected.

Table 3-6 (Cont'd.). Function of Front-Panel Controls, Indicators, and Monitor Jacks (Ref. Figure 3-3)

NAME	DESIGNATION	FUNCTION
DETECTOR Pushbutton Switch Assembly	A1S1	This switch assembly contains two interlocking pushbutton switches. Energizing the I/D switch matches the filter to a square PCM input signal - effectively simulating a reset-integrator detector. Energizing the F/S switch does not affect the filter characteristic which still effectively matches a pre-modulation-filtered bit stream. This position provides bit decision feedback for the NRZ codes only. A momentary-contact ENTER pushbutton switch enables the filter selection to be entered into static stores.
DETECTOR I/D, F/S Indicators	A2CR11, A2CR12 (LED's)	Displays the input detector mode selected.
DATA POLARITY Pushbutton Switch Assembly	A1S3	This switch assembly contains two interlocking pushbutton switches that provide selection of normal (NORM) or inverted (INV) input polarity. A momentary-contact ENTER pushbutton enables selected data to be entered into static stores.
DATA POLARITY NORM, INV Indicators	A2CR9, A2CR10, Light Emitting Diodes (LED's)	Display the input data polarity selected.
INPUT CODE Pushbutton Assembly	A1S2	Nine interlocking pushbutton switches that provide selection of NRZ-L, NRZ-M, NRZ-S, RZ, Biø-L, Biø-M, Biø-S, DM-M and DM-S codes. A momentary-contact ENTER pushbutton enables selected code to be entered into static stores.
INPUT CODE Indicators (LED's)	A2CR1 through A2CR8 and A2CR16	Displays the input code selected.

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

The theory of operation for the Model 720 is contained in the following paragraphs. The theory discussion is presented at two levels, general and detailed. The general theory is presented in paragraph 4.2, with reference to the simplified block diagram illustrated in Figure 4-1. The detailed theory of operation is provided in paragraph 4.3, with reference to detailed block diagrams, schematics, timing diagrams, and response curves.

4.2 GENERAL THEORY OF OPERATION

As shown in Figure 4-1, the bit synchronizer circuits may be divided into five basic functions: input conditioning, bit synchronization, data reconstruction, output conditioning, and program control. Each of these functions is described in the following paragraphs.

4.2.1 Input Conditioning

The input conditioning circuits (1) select the PCM input from one of four sources, (2) adjust the input signal amplitude, and (3) filter the input signal for application to the bit synchronization and data reconstruction circuits. Each of the circuits performing these functions is described below.

Selection of one of the four input sources is controlled by either the front-panel SOURCE switch or remote control, depending upon the operating mode selected. With the 720 in the LOCAL mode, input selection is controlled by the front-panel SOURCE switch. Setting the SOURCE switch to any number from one to four enables the corresponding input source line via the program control circuits. With the 720 in the OVERRIDE mode, the input source selection may be changed by using the SOURCE switch in conjunction with the source enter pushbutton. In REMOTE operation, the input source is selected by a computer (or similar remote device) via the program control circuits.

The AGC circuit enables the 720 to accept inputs ranging from 0.5V to 30.0V peak-to-peak without adjustment. The AGC circuit is basically a variable attenuator with attenuation varying from 1:1 to 6:1. The amount of attenuation provided by the AGC circuit is controlled by analog feedback from a difference amplifier in the DC restorer circuit. This signal represents the peak-to-peak level of the PCM input signal. The greater the amplitude of the feedback signal, the greater the attenuation of the PCM input signal. The configuration of the AGC circuit is such that the output can never exceed 5 volts peak-to-peak for PCM inputs up to 30 volts peak-to-peak. The AGC output is applied to the matched filter.

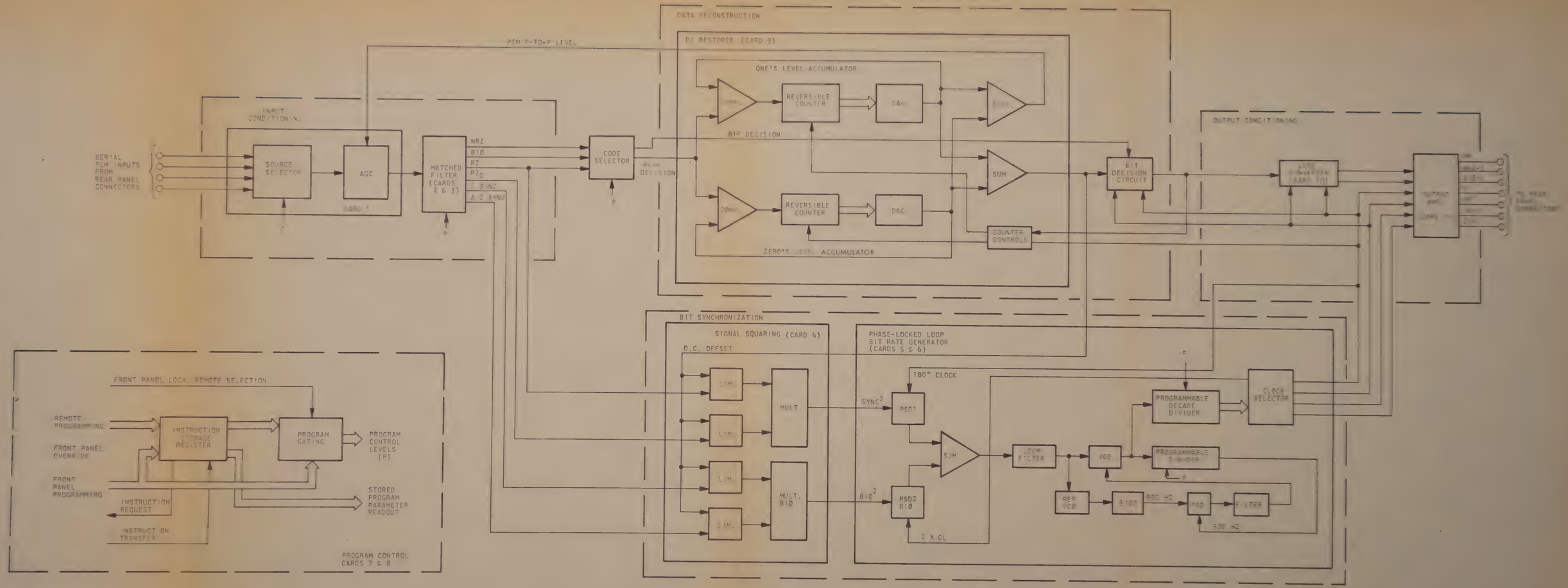


FIG 4-1
MODEL 720-02
SIMPLIFIED BLOCK DIAGRAM

The matched filter operates in conjunction with the bit decision circuit to provide a filter sample detector which approximates the reset integrator (integrate and dump) characteristic for NRZ codes. The matched filter consists of four RC low-pass filter sections (poles) and separate filter summing networks for processing RZ, NRZ, and Biø PCM inputs. For proper frequency response, the RC values in each filter section are determined either by the front-panel BIT RATE switches (in the LOCAL mode) or by the bit rate programmed from a remote source and entered into the program control circuits. By proper summation of the RC section outputs, the filter provides optimum outputs for the various code types and quadrature frequency components for use in the phase-locked loop. The matched filter outputs are applied to the bit synchronization and data reconstruction circuits.

4.2.2 Bit Synchronization

The bit synchronization circuit synchronizes the basic bit rate clocks (0°, 90°, 180°, and 270°, with respect to the PCM output) to the incoming PCM bit stream. This circuit consists of a signal squaring network and a phase-locked-loop bit rate generator.

The function of the signal-squaring circuit is to generate a signal representing the incoming bit rate for comparison with the internally generated bit rate clock. The operation of this circuit varies depending upon the PCM code type being received by the 720. For NRZ PCM inputs, the signal-squaring circuit limits the RZ and RZ delayed (RZ_D) outputs of the matched filter and multiplies the limiter outputs in an Exclusive-OR gate to generate the incoming bit rate ($SYNC^2$). When RZ PCM inputs are received by the 720, the RZ signal is the bit rate signal and is passed directly through the signal-squaring circuit to the phase-locked-loop bit rate generator. When processing either NRZ or RZ, the $Bi\emptyset^2$ output of the squaring circuit is inhibited. When the 720 is processing Biø inputs, both outputs ($SYNC^2$ and $Bi\emptyset^2$) of the squaring circuit are required to obtain bit synchronization. Because of bi-phase ambiguity, a string of bits at the same logic level could cause the bit rate clock to be 180° out-of-phase with the incoming signal if the $Bi\emptyset^2$ output alone was used to drive the phase-locked loop. However, the $SYNC^2$ signal detects a change of data state and this signal can be used in conjunction with $Bi\emptyset^2$ to drive the phase-locked loop.

The phase-locked-loop bit rate generator compares the incoming bit rate signal with the internally generated clock and, if a phase error is present, routes a correction signal to the internal VCO. The nominal clock frequency is programmed either at the front-panel BIT RATE switches (in LOCAL and OVERRIDE modes) or by a computer (in REMOTE mode). As with the squaring circuit, operation of the phase shift detector (PSD) and summing amplifier networks varies depending upon the PCM code type being received by the 720. For NRZ and RZ inputs, the $SYNC^2$ output is compared with the clock in one PSD. If a phase error exists between the two signals, an analog output from the summing amplifier represents this phase error. This signal is then amplified and filtered by the loop filter to provide an error signal that drives the VCO to the incoming bit rate. The loop filter is tunable (either locally at front panel or remotely by a computer) over the

entire bit rate range for filter bandwidths of 0.1%, 0.3%, and 1% of bit rate. The output voltage of the loop filter is sufficient to drive the VCO ± 10% of the bit rate; however, the tracking range is limited by gain changes in the phase-locked loop to ± 1%, ± 3%, and ± 10%, respectively, for the three filter bandwidths provided. For Biø inputs, the $SYNC^2$ output is compared with the clock and the $Biø^2$ output is compared with the twice bit rate clock (2XCL) in PSD1 and PSD2, respectively. The circuit gains are designed so that the PSD1 output will override the PSD2 output when random data is received. This resolves the Biø ambiguity that might result from phase locking with PSD2 alone. The 720 will then be held in phase by PSD2 over a long string of constant ONE's or ZERO's.

The output of the loop filter is applied to both the bit rate VCO and the reference VCO. The bit rate VCO is a free-running multivibrator which operates in the bit rate range of 8 MHz to 20 MHz. Programmable decade dividers enable this VCO to provide bit rate outputs from 1 bps to 5 Mbps. The reference VCO is a high-precision oscillator that operates at 50 kHz with no signal applied from the loop filter. Operation of the phase-locked loop is best described by considering circuit operation under two conditions. The first condition assumes that the incoming bit rate signal and the nominal bit rate frequency are in phase; that is, no error voltage is applied to the VCO's by the loop filter. The second condition assumes that the bit rate signals are out-of-phase and that an error voltage is applied to the VCO's. Each of these conditions is described below.

With no error output from the loop filter, the 50 kHz output of the high-precision reference VCO is divided by 100 and the resulting 500 Hz output is applied to one input of a phase shift detector in the phase-locked loop. Similarly, the bit rate VCO output is routed to a programmable divider. The programmable divider is designed so that, regardless of the nominal bit rate selected, the output of the programmable divider would also be 500 Hz, if the bit rate VCO were as accurate as the reference VCO. However, for high-frequency VCO's, this is not the case and the programmable divider output will vary from 500 Hz. This signal is applied to the second input of the phase shift detector. The PSD compares the two VCO outputs; the resulting error output is filtered and used to drive the bit rate VCO to the nominal bit rate selected.

Assuming the second condition, an error voltage output from the loop filter will deviate both VCO's. The reference VCO output is divided by 100 and the new reference frequency is applied to the PSD. The output from the bit rate VCO is divided in the programmable divider and routed to the second input of the PSD. From this point on, phase-locked-loop operation is as described in the preceding paragraph.

4.2.3 Data Reconstruction

The data reconstruction circuits consist of a DC restorer and a bit decision network. The function of the DC restorer is to continuously (bit-by-bit) determine the DC offset and the peak-to-peak value of the incoming PCM data. The DC offset is used as a reference signal by the bit decision network and by the signal squaring network in the bit synchronization circuit. The PCM peak-to-peak value

is fed back to the AGC circuit to control the AGC output. The operation of these networks is described in the following paragraphs.

The correct output of the matched filter is selected by the INPUT CODE selector and routed to the DC restorer and bit decision circuits. The DC restorer is composed of two high-speed logic level accumulators. One of these accumulators digitizes and stores the binary value of the voltage level corresponding to a logic ONE. The other accumulator digitizes and stores the binary value of the voltage level corresponding to a logic ZERO. The threshold for the bit decision is then set half-way between the two stored values.

The logic level accumulators used are the counter type, in which the direction of the reversible counter is controlled by the output of a comparator amplifier. One input to the comparator amplifier is the signal to be digitized, the other is the output of a digital-to-analog converter (DAC) reading the number stored in the reversible counter. If the input exceeds the stored number, the comparator will command the counter to count up; if the stored number exceeds the input, the comparator will command the counter to count down. The counter increments whenever it receives a clock pulse. The output of the bit decision circuitry steers the clock pulse to the ONE's counter at the center of a ONE bit and to the ZERO's counter at the center of a ZERO bit, thus permitting each converter to increment and store the number corresponding to the positive and negative input levels. The rate of counting and the resolution of each DAC are selected to permit the counter to follow baseline variations of the input signal at rates exceeding 0.1% of the bit rate, while at the same time averaging out the variations from superimposed white noise.

The outputs of the two DAC's are summed in a resistive network, and that sum is used as a reference both for the bit decision limiter and the limiters supplying signals to the phase-locked-loop squaring limiters. The use of the digital DC restorer and high-gain low-drift limiters ensures that the bit decision does not favor a ONE or a ZERO with both balanced and unbalanced input PCM wavetrains.

4.2.4 Output Conditioning

The bit decision output is routed to the code converter and output amplifier circuitry. The code converter converts any of the IRIG codes to NRZL for the decommutator output, and also converts the NRZ to BiØL and DM for the tape recorder output. The output amplifiers provided are discrete component circuits designed for driving terminated coaxial cables.

4.2.5 Program Control

Program control (paragraph 3.2) is selected by the LOCAL/REMOTE/OVERRIDE switch on the front panel. This switch controls the operation of the program control cards (Bit Rate Store and Format Store) as described below.

In the LOCAL mode, the signal lines from the front-panel switches are selected by a set of solid-state multiplexers and directly drive the program control lines. In the REMOTE and OVERRIDE modes, these same multiplexers select the outputs of the storage registers on the program control cards rather than the front-panel switches. These storage registers can be loaded (1) by a computer or similar device when the 720 is in the REMOTE mode, or (2) by the front-panel switches when the 720 is in the OVERRIDE mode. In both REMOTE or OVERRIDE modes, the outputs of the program storage registers control the 720 operation, only the method of loading the stores differs. Consequently, two completely independent programs can be set into the 720. One program is stored in the front-panel switch positions, and the other is stored in the program control card storage registers. Either program can be selected by the REMOTE/LOCAL/OVERRIDE switch.

4.3 DETAILED THEORY OF OPERATION

The detailed theory of operation is presented in the following paragraphs at the functional card level. In addition to the detailed card schematics in Section 5, simplified card schematics are provided for the more complex functional cards.

4.3.1 Input Source Select Card 1 (Figure 5-10)

4.3.1.1 Input Source Select Circuit

Selection of one of the four input sources is controlled by three BCD (4-2-1) input lines from the program control cards (Bit Rate and Format Store Cards 7 and 8). The three lines are decoded in a BCD-to-decimal decoder and the four decimal output lines are routed to dual-element light-emitting-diode (LED)/photoresistor devices (RT3 through RT6) which act as switches on the input source lines.

When processing RZ or NRZ at bit rates below 100 bps, the logic level at pin 24 (1-99 BITS) falls to a ZERO. This signal turns on RT1 to enable the selected PCM input signal to bypass the parallel capacitors C16 and C17. For Bi∅ and DM inputs less than 100 bps and for all PCM code inputs greater than 100 bps, the level at pin 24 is at logic ONE and capacitors C16 and C17 provide AC coupling of the input.

As shown in Figure 5-10, jumper terminals are provided on each of the four input signal lines. These jumper connections may be used for termination of input signals as required. Normally, 100-ohm termination resistors are supplied.

4.3.1.2 AGC Circuit

The AGC circuit enables the Model 720 to accept inputs from 0.5V to 30.0V in amplitude without adjustment. The AGC circuit consists of a fixed attenuator, a variable attenuator, and an output amplifier stage. The fixed attenuator divides the amplitude of the input signal by 2; the attenuation of the variable attenuator varies from 1:1 to a maximum attenuation of 6:1 of the input signal amplitude. The output amplifier stage has a gain of 2. The amount of attenuation

provided by the variable attenuator is controlled by analog feedback from a difference amplifier driven by the positive and negative DAC outputs from DC Restorer Card 9. This signal represents the peak-to-peak level of the conditioned PCM signal. The greater the amplitude of this signal, the greater the attenuation of the incoming PCM signal. After attenuation, the PCM signal is amplified by a gain of 4 in Q4 and applied to the input of the matched filter. The configuration of the AGC circuit is such that the output can never exceed 5 volts for PCM inputs up to 30 volts peak-to-peak.

4.3.1.3 Input Status Signals

In addition to the source select and AGC circuits, card 1 also contains circuits that furnish input status signals to the front panel and to external equipment. The analog output of differential amplifier U3, representing the PCM peak-to-peak level from the DC restorer, is checked (1) for amplitudes exceeding 20 volts (INPUT HI), (2) for amplitudes of 0.6V or less (INPUT LO), and (3) for amplitudes of approximately 300 millivolts or less (SIGNAL LOSS). If any of these conditions exist, a logic ONE level is present on the corresponding status output line. The INPUT HI, INPUT LO, lines are brought out to the rear panel for use by external equipment. A logic ONE on the SIGNAL LOSS line turns on front-panel SIG LOSS indicator. The ZERO output is routed to the phase detector on Loop Filter Card 5 and is used for clamping the loop to center frequency when loss of signal occurs. The output of difference amplifier U3 is also used to drive the front-panel INPUT meter which displays the input signal level in volts peak-to-peak.

4.3.2 Matched Filter and Signal Squaring Circuits Cards 2, 3, and 4 (Figures 4-2, 5-12, 5-14, and 5-16)

4.3.2.1 General Signal Flow

The matched filter is located on Input Filter Cards 2 and 3, and Filter Control Card 4. As shown in the simplified schematic diagram (Figure 4-2), the Input Filter Cards 2 and 3 contain four RC low-pass filter sections (poles) driven by extremely low-drift, wideband amplifiers.

Tuning of the RC sections is controlled by the programmed bit rate. Filter Control Card 4 receives bit rate and bit rate multiplier inputs (Figure 5-16, sheets 3 and 4) from Bit Rate Stores Card 7 and Format Stores Card 8, respectively. The Filter Control Card performs BCD-to-binary conversion on the bit rate inputs and the resulting signals ($\overline{\text{BBR1}}$ through $\overline{\text{BBR7}}$) control transistor switches that switch the proper resistors for each pole into the circuit. The Filter Control Card also performs BCD-to-decimal conversion on the bit rate multiplier inputs and the resulting signals ($\overline{\text{1B}}$, $\overline{\text{10B}}$, $\overline{\text{100B}}$, etc.) control transistor switches and, in the case of the megabit ($\overline{\text{MB}}$) multiplier, relay K1 (Figure 5-14, sheet 1), that switch the proper capacitors for each RC section into the circuit.

Separate summing amplifiers (U1 and U5 on Card 3) are provided to generate a matched filter response for NRZ and Biø inputs. When RZ is the input PCM

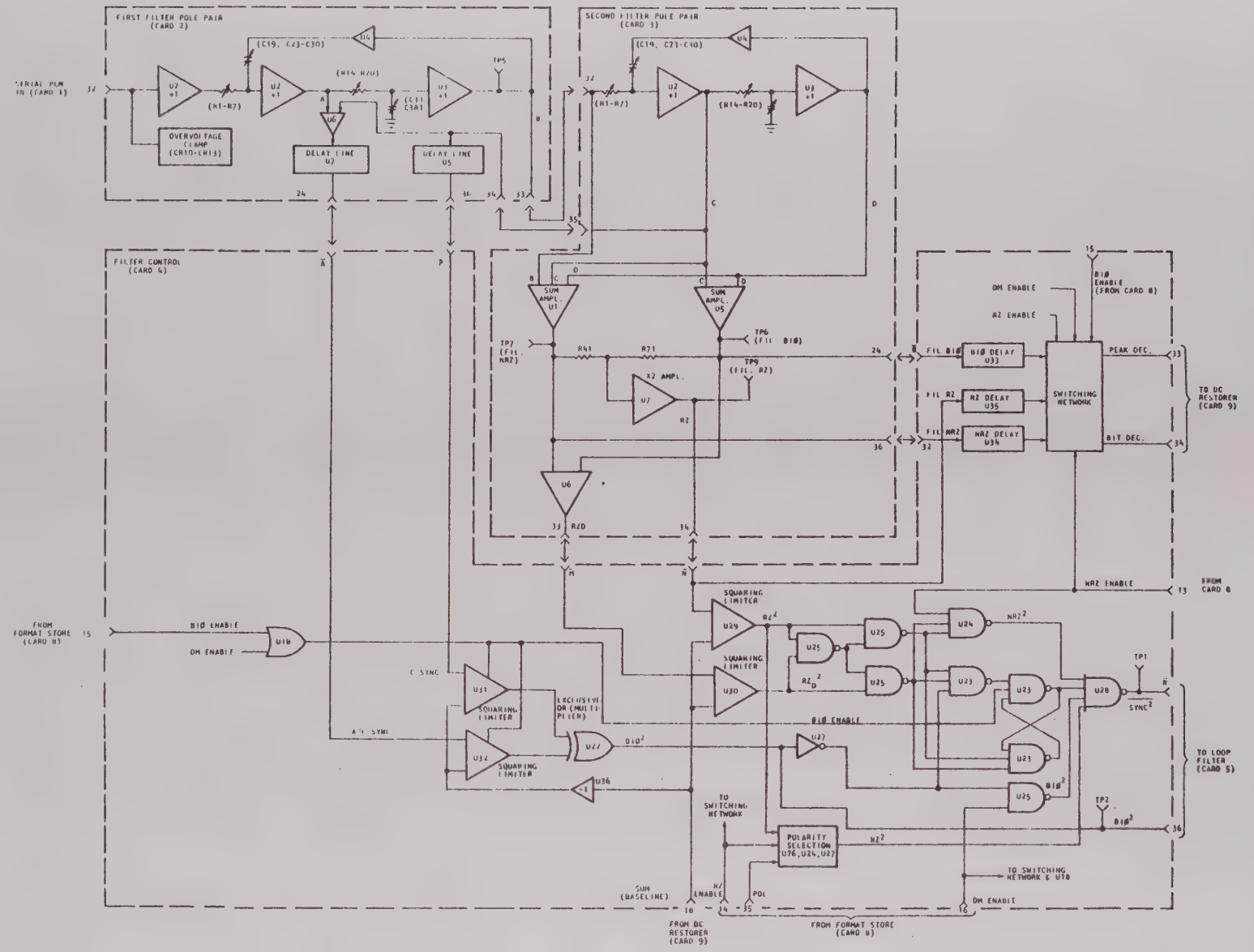


Figure 4-2. Simplified Schematic of Matched Filter and Signal Squaring Circuits

code, the outputs of the same summing amplifiers used for NRZ and Biø are summed at U7 to derive the matched RZ response, and subtracted at U6 to derive the RZ delayed (RZ_D) response. When DM-M or DM-S is the input PCM code, the RZ out of U6 is the desired response. These signals are routed to delay networks which compensate for other delays in the signals which drive the phase-lock loop. Outputs from the delay circuits are routed to a switching network and are switched to the peak decision (PEAK DEC) and bit decision (BIT DEC) output lines as follows:

a. When NRZ is the 720 input code, the filtered NRZ (FIL NRZ) signal is switched to both the PEAK DEC and BIT DEC output lines.

b. When Biø is the 720 input code, the filtered Biø (FIL Biø) is routed to the BIT DEC line and filtered RZ is routed to the PEAK DEC line.

c. When RZ or DM is the 720 input code, filtered RZ is routed to both lines.

The BIT DEC and PEAK DEC outputs are routed to DC Restorer Card 9.

The RZ and RZ_D outputs are also routed to squaring limiters U29 and U30 on Filter Control Card 4. The outputs of the squaring limiters are used to generate $SYNC^2$, a timing signal with a frequency component at the incoming bit rate. This signal is used (at Loop Filter Card 5) to synchronize the internal clock with the incoming PCM wave train.

The C pole output of Card 3 is routed to delay circuit U5 of Card 2 and is also summed with the A pole output and applied to delay circuit U7. The delay circuit outputs (C SYNC and A/C SYNC) are routed through squaring limiters U31 and U32 and exclusive-OR U22 to generate $Bi\emptyset^2$. When the 720 is receiving Biø inputs, $Bi\emptyset^2$ is used (by Loop Filter Card 5) in addition to $SYNC^2$ to synchronize the internal clock with the Biø wave train. When the 720 is receiving DM inputs, $Bi\emptyset^2$ is used instead of $SYNC^2$ (by Loop Filter Card 5) to synchronize the internal 2-times-clock signal with the incoming DM wave train.

The preceding paragraphs described general signal flow through the matched filter and squaring circuits contained on Cards 2, 3, and 4. Paragraphs 4.3.2.2 through 4.3.2.5 describe operation of these circuits when processing each of the four input code types (NRZ, RZ, Biø, and DM).

4.3.2.2 Matched Filter Operation for Square PCM NRZ Inputs

The square PCM NRZ input from the AGC circuit (Card 1) is applied to the four-pole filter contained on Filter Cards 2 and 3. For proper frequency response,

the RC values in each filter section are determined by the program control lines from Cards 7 and 8 (paragraph 4.3.2.1). RC components are selected to maintain filter response over the entire bit rate range (1 bps to 5 Mbps).

Figure 4-3 illustrates the response curve of the filter at the NRZ output port. For optimum signal-to-noise performance, it is desired to pass the fundamental and odd harmonics of the spectrum and to reject the even harmonics. The response curve illustrates this "notching" function performed by the matched filter for square PCM NRZ inputs. The outputs of filter sections B, C, and D are applied to operational summing amplifier U1 and the resulting filtered output is the same waveform that would result if the reset integrator method of filtering were used. However, the matched filter is linear and independent of bit synchronizer timing. Because of this fact, the matched filter is not subject to timing errors inherent in the reset integrator method when operating at high bit rates.

The filtered NRZ is routed through delay U34 to the switching network where a logic ONE NRZ enable input from Format Store Card 8 switches the filtered NRZ to the BIT DEC and PEAK DEC output lines. The signal is routed on these lines to the DC restorer and bit decision circuits on Card 9.

Simultaneously, a timing signal with a frequency component at the bit rate must be generated to synchronize the internal clock with the incoming NRZ wave train. This timing signal ($SYNC^2$) is generated in the following manner. The outputs of summing amplifiers U1 and U5 are added in a resistive network; and routed through a X2 amplifier (U7) to one input of differential limiter U29. The outputs of U1 and U5 are also routed to amplifier U6 where they are subtracted, resulting in a waveform delayed 1/2-bit time from the input to U29. This waveform is applied to one input of differential limiter U30. The second (differential) input to U29 and U30 is obtained from the summing amplifier in the DC restorer. This input ensures optimum threshold levels for all code patterns. The limiter outputs are multiplied in an exclusive-OR circuit (U25-U24) and the resulting NRZ^2 timing chain is routed to NAND-gate U28. The other inputs to U28 are at logic ONE levels and the $SYNC^2$ output of U28 is the inversion of the NRZ^2 timing chain. $SYNC^2$ is routed to a phase shift detector in Loop Filter Card 5.

4.3.2.3 Matched Filter Operation With Square RZ Inputs

When square-sided RZ is the input to the matched filter, the filter frequency response shown in Figure 4-4 is desired. This response is available at the RZ output port of the filter. Filter operation for square RZ inputs is similar to that described for processing square NRZ inputs. The signal is filtered in the four low-pass RC sections and the low-pass pole outputs are applied to the summing amplifiers U1 and U5, which generate the NRZ and Biø matched filter responses, respectively. The RZ matched filter response is generated by summing the NRZ and Biø responses in resistors R41 and R71 (Card 4). The filtered RZ signal is then routed through the X2 amplifier via delay U35 and the switching network to the DC restorer. The output of the X2 amplifier is also routed to one input of differential comparator U29. The other input to the comparator is the

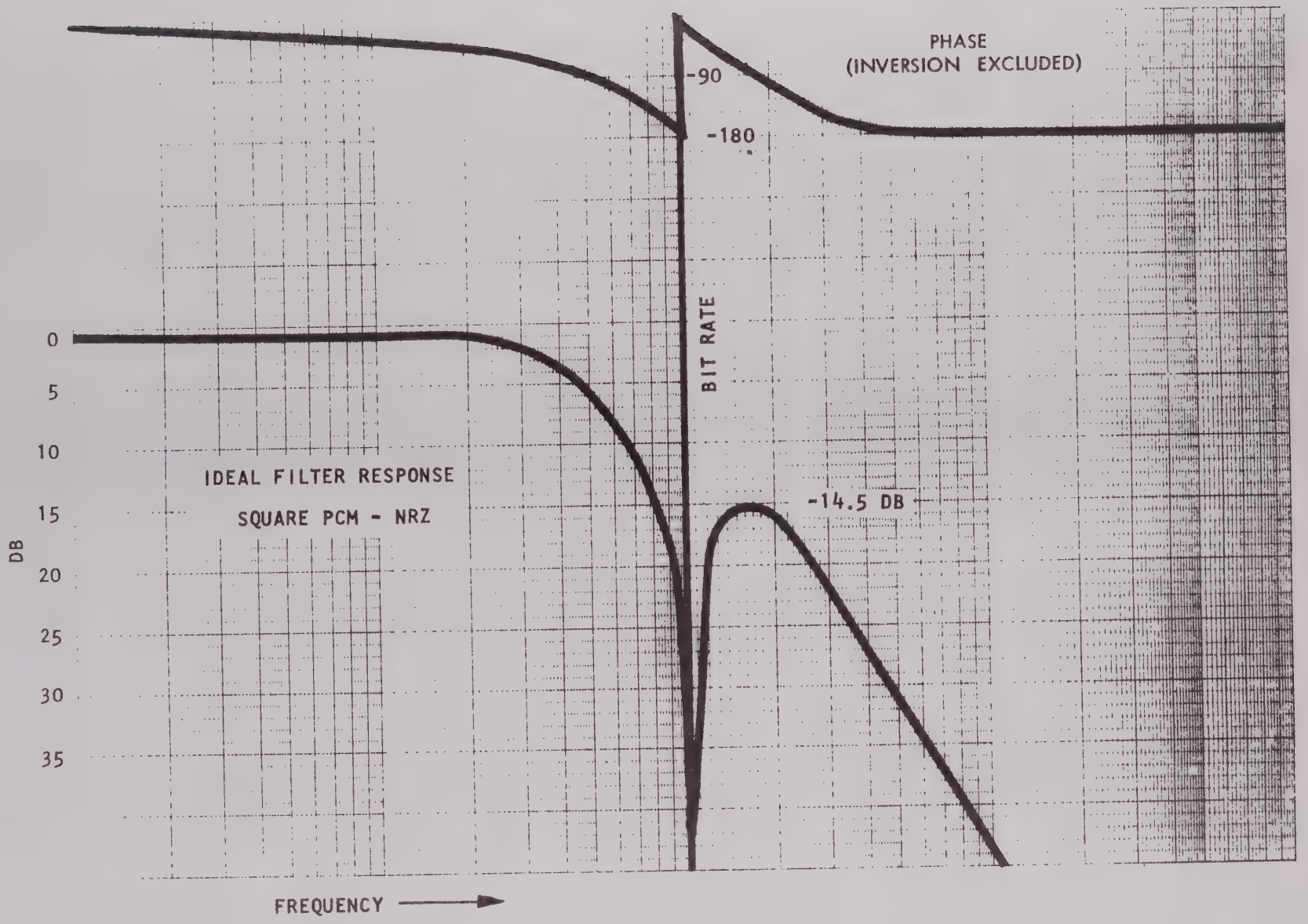


Figure 4-3. Ideal Filter Response for Square PCM NRZ

"sum" output of the DC restorer, which represents the baseline of the PCM signal. The squaring process (required to generate input timing when processing NRZ) is not required when processing RZ because the RZ signal has a fundamental component at the bit rate. The RZ signal is limited and passed through the polarity selection circuit and U28 to Loop Filter Card 5.

4.3.2.4 Matched Filter Operation With DM Inputs

When DM-M or DM-S is the input to the matched filter, the filter frequency response, shown in Figure 4-4, is desired.

Generation of the PEAK DEC and BIT DEC outputs is identical to that described for RZ inputs (paragraph 4.3.2.2). The reference timing signal ($\overline{\text{SYNC}^2}$) is generated in the following manner. The DM enable input from Format Stores Card 8 enables C SYNC and A/C SYNC to generate the Bi$\emptyset^2$ output of exclusive-OR U22. This signal is gated through NAND-gate U25 (by DM ENABLE) to generate $\overline{\text{SYNC}^2}$ at the U28 output. The Bi$\emptyset^2$ output at pin 36 is inhibited at Phase Shift Detector 2 on Loop Filter Card 5.

4.3.2.5 Matched Filter Operation With Bi$\emptyset$ Inputs

When PCM Bi$\emptyset$ is the input, the filter response desired is shown in Figure 4-5. The summation of the proper low-pass poles in U5 generates this response. The output of U5 is the Bi$\emptyset$ output port of the filter and is routed via Bi$\emptyset$ delay U33 and the switching network as the BIT DEC input to DC Restorer Card 9. This signal cannot be used for DC restoration because it does not contain a DC component. However, the output of the RZ filter port contains the required DC component and this signal is routed via RZ delay U35 and the switching network as the PEAK DEC input to DC Restorer Card 9.

Two pulse trains (referenced to the incoming Bi$\emptyset$) are generated to sync the internal bit rate clocks with the incoming Bi$\emptyset$. (In processing NRZ, RZ, or DM, a single clock, referenced to the PCM input is required to sync the internal bit synchronizer clock with the incoming PCM data.) However, in the processing of Bi$\emptyset$ data, the problem of Bi$\emptyset$ ambiguity must be reconciled. A constant bit stream of logic ONE's (or ZERO's) could cause the internal bit synchronizer clock to be 180° out of phase with the incoming Bi$\emptyset$ data, if the Bi$\emptyset^2$ output (generated by exclusive-OR U22) were used by itself to drive the phase-locked-loop bit rate generator.

However, the $\overline{\text{SYNC}^2}$ signal contains the true clock information whenever a change of data state (logic ZERO to logic ONE and vice versa) occurs. This signal is used in conjunction with the Bi$\emptyset^2$ output to drive the phase-locked loop. The $\overline{\text{SYNC}^2}$ signal is routed to one phase shift detector in the loop filter (PSD) and the Bi$\emptyset^2$ signal is applied to the other PSD. These signals are generated in the following manner.

The Bi$\emptyset^2$ output is generated by squaring and limiting C SYNC and A/C SYNC at U31 and U32, respectively, and then routing these signals to exclusive-OR U22. The Bi$\emptyset^2$ signal is routed to a PSD on the Loop Filter Card 5 via card connector pin 36.

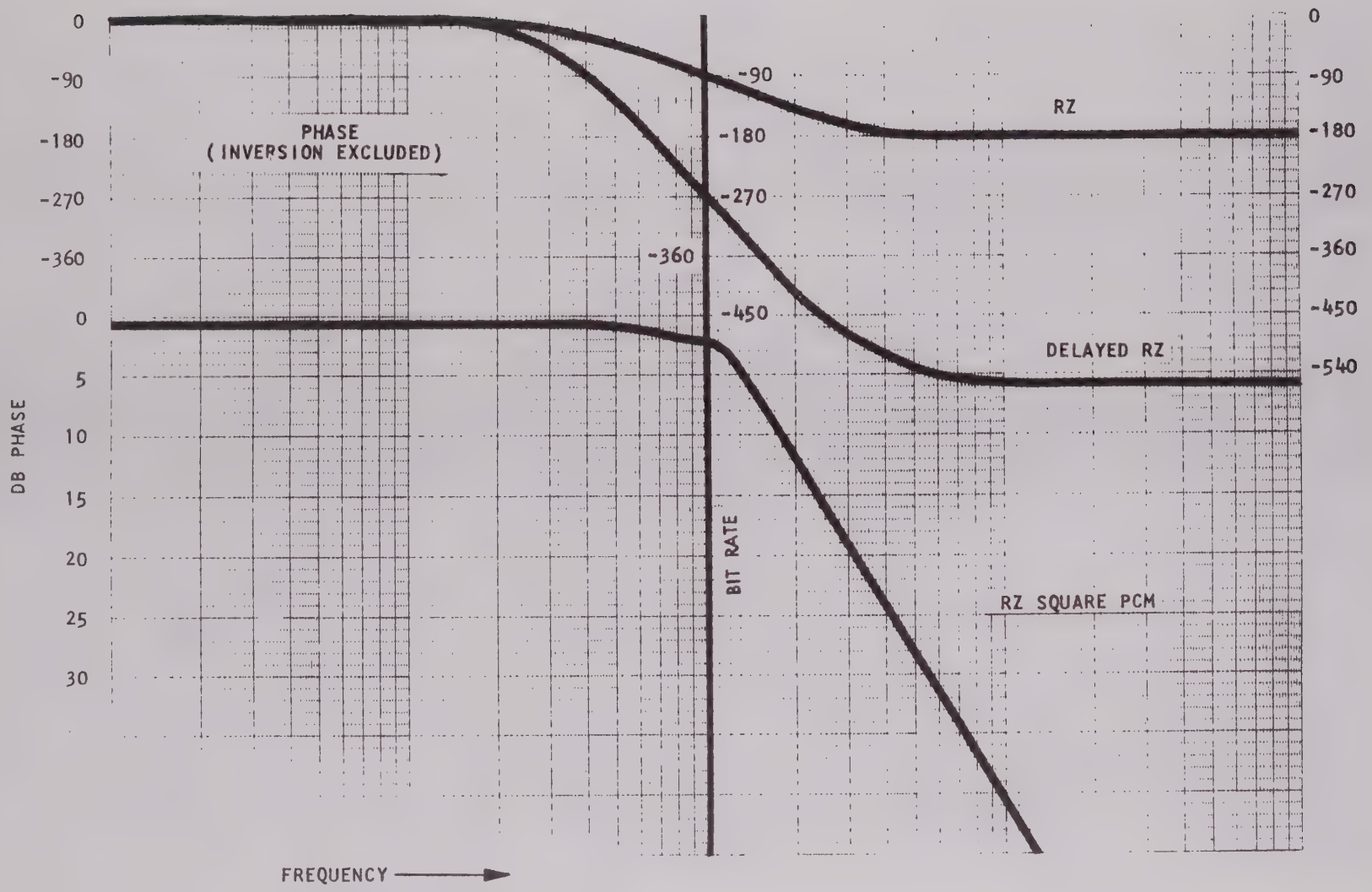


Figure 4-4. Ideal Filter Response for Square PCM RZ and DM Inputs

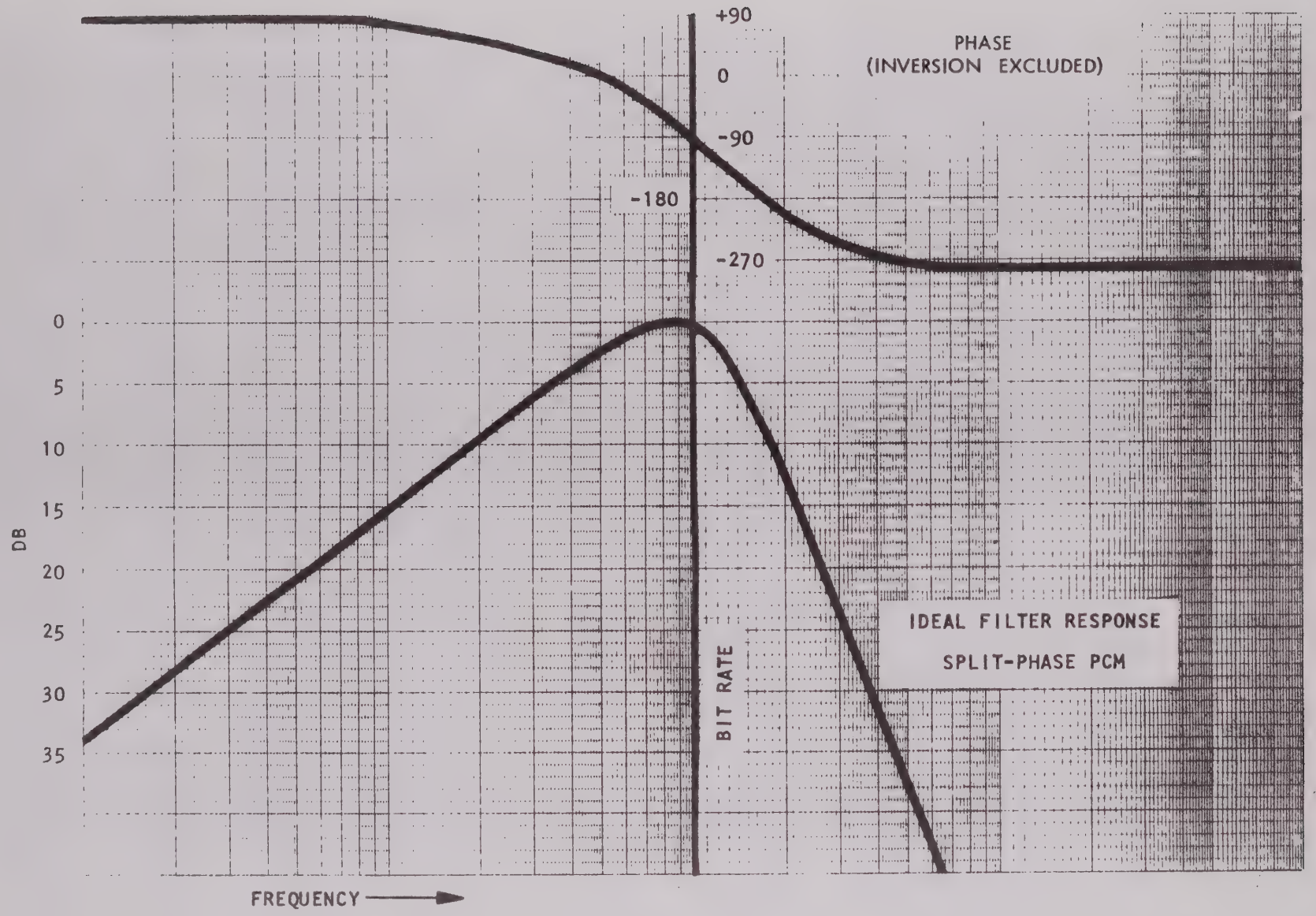


Figure 4-5. Ideal Filter Response for PCM Biø

The $\overline{SYNC^2}$ output is generated by using $\overline{Bi\emptyset^2}$ to gate $\overline{NRZ^2}$ through circuit U23 which consists of a NAND-gate and a cross-coupled flip-flop. The U23 output is inverted and routed as $SYNC^2$ to a second PSD on Loop Filter Card 5.

4.3.3 Phase-Locked-Loop Filter Card 5 (Figures 4-6 and 4-7)

4.3.3.1 General Signal Flow

Operation of the phase-locked-loop (PLL) filter when the 720 is processing NRZ, RZ or DM inputs is almost identical. In each case, the nominal bit rate (twice bit rate) for DM generated by the phase-locked-loop VCO on Card 6 is compared with the $SYNC^2$ output from Filter Control Card 4 to determine the phase difference (if any) between the nominal VCO clock and the bit rate component of the $SYNC^2$ signal. If a phase difference is detected, loop amplifier/filter circuits provide an analog voltage (DEV) equivalent to the phase error and this signal drives the VCO to null out the phase error.

When the 720 is processing Bi$\emptyset$ inputs, the $Bi\emptyset^2$ input from Filter Control Card 4 is simultaneously compared in a second phase detector with the twice clock (2XCL) input from VCO Card 6. This phase detector output is summed with the $SYNC^2$/CLK3 phase detector output and applied to the loop amplifier/filter circuits. Operation of the loop amplifier/filter circuits is as described in the preceding paragraph.

PLL filter operation for each 720 PCM input code is described in the following paragraphs. Figures 4-6, 4-7, and the detailed schematic, Figure 5-18, should be used with the discussion.

4.3.3.2 PLL Filter Operation With RZ and NRZ Inputs

As shown in Figure 4-6, $\overline{SYNC^2}$ and $\overline{XCL\ EN}$ are applied to NAND-gate U5B. $\overline{XCL\ EN}$ remains at a logic ONE level at all times except when an external clock input (XCL) is used by the 720. With $\overline{XCL\ EN}$ at ONE, the $SYNC^2$ input is inverted in U5B and applied to Phase Shift Detector (PSD) 1. The $\overline{ZERO\ SIG}$ input from Card 1 is also applied to PSD1. [At any time the $\overline{ZERO\ SIG}$ drops to logic ZERO (indicating input signal loss), the PLL filter operation is inhibited.] The remaining input to PSD1 is the CLK3 output from VCO Card 6. Before application to PSD1, CLK3 is passed through a clock symmetry adjustment circuit (CR16, CR17, R89, and R90) which ensures clock symmetry at high bit rates.

PSD1 compares the $SYNC^2$ and CLK3 inputs to detect any phase difference between the two signals. (A phase difference of 90° between the two signals is recognized as zero phase error.)

If zero phase error exists, the output waveforms of PSD1, the current switch, and the V_o input to the loop filter are as shown in Figure 4-7 (A). Because of the zero phase error condition, the V_o tri-level output is symmetrical and has a DC component of zero. This signal is passed through the loop filter to provide a correction voltage output (DEV) to the VCO Card.

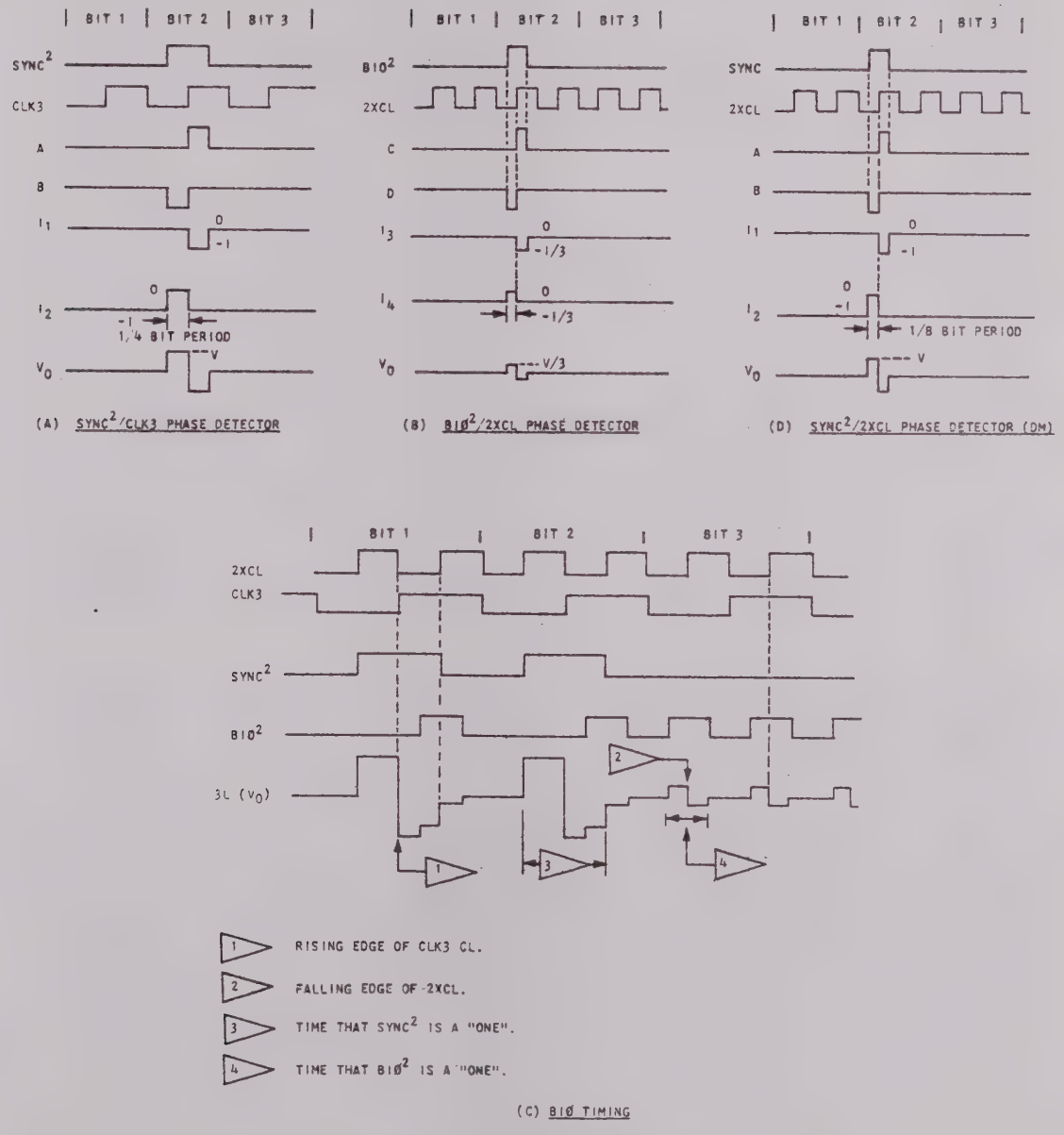


Figure 4-7. Timing Diagrams for Phase-Locked-Loop Filter Operation

If PSD1 recognizes any deviation from zero phase error, the V_o output becomes nonsymmetrical in either the positive or negative direction. This signal is applied to the loop filter which consists basically of a low-pass filter circuit, a high-pass filter circuit, summing resistors that sum the outputs from the two filter networks and an output buffer amplifier.

Operation of the low-pass and high-pass filter circuits is as follows.

V_o is applied to the low-pass filter consisting of R1 and C1, C2 or C3. The capacitor selected is determined by the programmed loop width. The low-pass filter removes the high frequency components of V_o which would otherwise cause DC offset in high-gain amplifier U9 due to rectification of the fast edges of the input signal.

The filtered input is applied to operational amplifier U9. The components selected for the U9 feedback loop are determined by the programmed loop width and bit rate. The capacitors in the feedback loop are arranged in three groups, with five capacitors to the group. The loop width programmed (wide, medium or narrow) determines the capacitor group connected into the feedback loop. Selection of capacitors within each group is controlled by the bit rate multiplier decades. (This method provides great flexibility in satisfying customer requirements.) Selection of RT1 through RT5 in the feedback loop is controlled by the bit rate (5 bits binary) programmed. Attenuators R27 and R28 are switched into the feedback circuit when medium and narrow loop widths, respectively, are programmed. Inserting these resistors into the feedback loop enables reduction of the loop width while maintaining a constant damping factor. Regardless of the loop width selected, the DC gain (from the input of U9) of the signal applied to summing resistor R25 is 100.

In the high-pass filter, V_o is buffered by U10 and filtered by a high-pass filter consisting of capacitor C18 and R16, R17 or R18. The resistor selected is controlled by the programmed loop width. The high-pass filtered output is summed with the low frequency output at summing resistors R18 and R25. The summing node then contains a "tri-level" signal with square edges. The function of the high-pass path is to re-insert the high frequency components that were removed by the R_1/C_1, C_2, C_3 filter. In effect, the high frequencies have been by-passed around the high gain Loop Amplifier (U9), and are available to the VCO to assist acquisition performance. The resulting tri-level output is low-pass filtered by an RC output filter consisting of R19 and capacitors selected from C21 through C26 by the programmed bit rate multiplier. This low-pass filter partially integrates the tri-level pulse to avoid overdriving the VCO, while passing enough high frequency energy to provide fast acquisition.

4.3.3.3 PLL Operation With DM Inputs

Operation of the PLL with DM inputs is the same as that described for RZ and NRZ with the exception that the $SYNC^2$ input is compared with the 2XCL clock input from VCO Card 6. The waveforms for PLL operation with DM inputs are shown in Figure 4-7 (D).

4.3.3.4 PLL Filter Operation With Biø Inputs

When the Model 720 is receiving Biø inputs, PSD1 operates as previously described and, in addition, PSD2 is used to detect a phase error between the $Bi\emptyset^2$ data rate signal and the internal twice clock (2XCL) signal. The waveforms for PSD2 operation are shown in Figure 4-7 (B). Figure 4-7 (C) illustrates the V_o multi-level waveform developed when both PSD's are in operation. The use of both PSD's is required (1) to resolve the Biø ambiguity problem and (2) to maintain bit synchronization during periods when the incoming bit pattern is a stream of constant ONE's or ZERO's. When the 720 receives a random data pattern, PSD1 overrides PSD2 and supplies a correction voltage through the PLL filter to the VCO, ensuring a correct phase lock. This override is a result of the 3 to 1 ratio of the output currents of PSD1 and PSD2. However, when the incoming bit pattern changes from a random data pattern to a period of constant ONE's or ZERO's, PSD2 supplies sufficient phase information to hold phase lock. In effect, the random data transitions between streams of constant ONE's or ZERO's enables PSD1 to drive the VCO into sync. During the period of constant ONE's or ZERO's or reduced data transitions, PSD2 provides phase information to hold the loop in sync.

4.3.3.5 PLL Operation Using an External Clock Input

When an external clock is used with the 720 input, the $\overline{SYNC^2}$ and $Bi\emptyset^2$ inputs to the PLL are not needed because the external clock (XCL) is compared with the internal clock (CLK3 for all input codes except DM; 2XCL for DM codes). When XCL is used, the logic ZERO $\overline{XCL\ EN}$ inhibits the $SYNC^2$ input to PSD1 and also inhibits the $Bi\emptyset^2$ input to PSD2. The external clock capability is provided for special purpose or bench testing configurations where it is useful to "hardwire synchronize" the 720 to a clock signal. The 720 loop actually phase locks to the external clock in this case. The phase relationship is such that the external clock (XCL) leads the 720's CLK3 by 90°. (For a DM code input, the XCL must be at twice the bit rate, and it leads the 720's 2XCL by 90°.) The phase relationship between the XCL and the input PCM should be as follows:

1. NRZ, RZ, or Biø-L Inputs: The XCL should be a 90° clock with respect to the PCM bit stream.

2. Biø-M or S Inputs: The XCL should be a 270° clock with respect to the PCM stream.

3. DM Codes: The XCL should be a 2XCL with positive-going transitions at the beginning of the bit period.

4.3.4 Phase-Locked-Loop VCO Card 6 (Figure 4-8)

The PLL filter output (modulation input) is applied to both the high frequency VCO (Q4, Q5, Q7, and Q8) and the 50-kHz reference oscillator (U15, U18). The high frequency VCO is a free-running multivibrator that operates in the bit rate range of 8 MHz to 20 MHz. The reference oscillator is a high precision

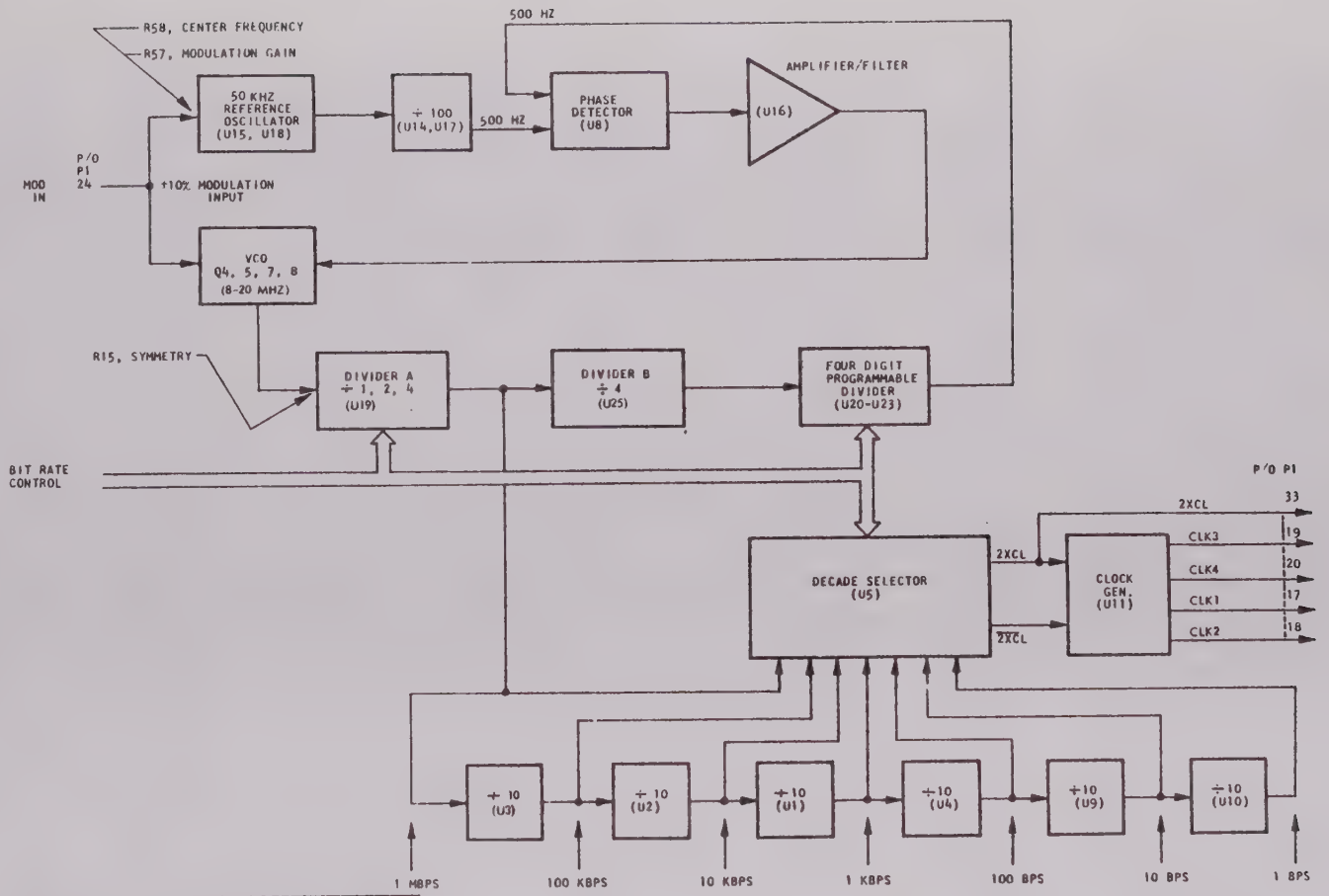
oscillator that provides a 50-kHz output with a 0V modulation input from the PLL filter.

The bit rate output of the VCO card is determined by the bit rate control inputs driven by the program control lines from cards 7 and 8. These control inputs are applied to the programmable dividers (divider A and four-digit programmable divider U20-U23) and to the decade selector in the following manner. The bit rate and multiplier control inputs determine whether divider A functions as a ÷1, ÷2, or ÷4 circuit. The multiplier control input also controls decade selection. The four bit rate digits control the four-digit programmable divider U20-U23. The table in Figure 4-8 provides examples of divider A functions and the associated 2XCL and VCO frequency for selected bit rates above and below 1 Mbps.

Assuming a 0V modulation input (no error output from the loop filter), the 50 kHz output of the reference oscillator is divided by 100 at U14, U17 to provide a 500 Hz input to phase/frequency comparator U8. The high frequency VCO output is routed through divider A, divider B, and the four-digit programmable divider (which is programmed by the four bit rate digits to divide by a number between 1000 and 9999). The programmable divider output is routed to U8 where it is compared with the 500 Hz reference frequency. The output from U8 is filtered and amplified in U16 and fed back to the high frequency VCO to close the loop. As a result, both frequency inputs to U8 are maintained at 500 Hz, and the output of the high frequency VCO is maintained at the correct frequency to generate the selected bit rate. The output of divider A is routed to the decade dividers that feed the programmed decade selector. The outputs of decade selector U5 are the twice bit rate clock (2XCL) and its complement ($\overline{2XCL}$). These signals are used by clock generator U11 to derive the CLK1, CLK2, CLK3, and CLK4 bit rate clocks. The 2XCL is also routed to pin 33 of the card connector for use by the Phase-Locked-Loop Filter Card 5 and $\overline{2XCL}$ is routed to pin 32 of the card connector for use by Code Converter Card 10.

If a phase error voltage (modulation input) is received from the phase-locked-loop filter card, both the high frequency VCO and the 50 kHz reference oscillator are deviated. As previously described, the reference oscillator output is divided by 100 at U14, U17, and applied to one input of phase detector U8 and the VCO output is divided down and applied to the second input of U8. When the VCO is operating, these two inputs to U8 are in phase and the output of amplifier/filter U16 remains constant at the value that provides the correct center frequency.

When the modulation input (described in the preceding paragraphs) occurs to drive the VCO off center frequency, it is applied to both the reference VCO and the high frequency VCO simultaneously, so that both are deviated exactly the same percentage. This technique is required in order to maintain the two inputs to U8 at the same frequency and phase. When this is done, the output of U16, which controls the "coarse tuning" or "center frequency" tuning of the high frequency VCO, remains constant. At the same time, the modulation input controls the "fine tuning" input of the high frequency VCO and drives it in the correct direction to track the incoming bit rate.



BIT RATE	2XCL	DIV A	VCO FREQ.	
1 MBPS	2.0 MHZ	÷4	8.0 MHZ	ABOVE 1 MBPS
1 MBPS	4.0 MHZ	2	8.0 MHZ	
3 MBPS	6.0 MHZ	2	12.0 MHZ	
4 MBPS	8.0 MHZ	1	8.0 MHZ	
5 MBPS	10.0 MHZ	1	10.0 MHZ	
1 KBPS	2.0 KHZ	4	8.0 MHZ	BELOW 1 MBPS
2 KBPS	4.0 KHZ	2	8.0 MHZ	
3 KBPS	6.0 KHZ	2	12.0 MHZ	
4 KBPS	8.0 KHZ	1	16.0 MHZ	
5 KBPS	10.0 KHZ	1	10.0 MHZ	
6 KBPS	12.0 KHZ	1	12.0 MHZ	
7 KBPS	14.0 KHZ	1	14.0 MHZ	
8 KBPS	16.0 KHZ	1	16.0 MHZ	
9 KBPS	18.0 KHZ	1	18.0 MHZ	

Figure 4-8. Simplified Schematic of Phase-Locked-Loop VCO

4.3.5 Bit Rate Store Card 7 (Figure 5-22)

This card consists of data selection circuits, storage registers, and output gating circuits that store the selected four-digit bit rate and present this parameter on output lines (program control lines) for programming the 720 logic circuits. The bit rate is programmed in either the LOCAL or REMOTE mode. In addition, a bit rate selected in the REMOTE mode can be modified at the 720 front panel by depressing the OVERRIDE pushbutton and entering the desired bit rate at the front-panel switches. Because the circuits for storing and outputting each bit rate digit are functionally identical, only one of these circuits (the MSD bit rate store) is described below. Circuit operation is discussed for the LOCAL, REMOTE, and OVERRIDE modes.

The circuit for selecting and storing the MSD of the bit rate consists of integrated circuits (IC's) U1 and U7. The remote MSD inputs (in BCD 8-4-2-1) are applied to U1. The LOCAL MSD inputs (also in BCD 8-4-2-1) are applied to both U1 and U7.

As shown in Figure 5-22, U7 is a multiplexer that selects either the LOCAL (front panel) bit rate input or the output of U1. When the front-panel mode switch is set to LOCAL, the A/B ENABLE input to U7 is a logic ONE and the four switches in U7 route BR 1-1, -2, -4, and -8 to the output lines of U7.

With the mode switch set to REMOTE, the remotely programmed MSD of the bit rate (RMTIN 5 - RMTIN 8) is selected and clocked into storage as follows: A ZERO at $\overline{\text{REMOTE}}$ enables U11, a one-of-16-line decoder which decodes the MODULE ADDRESS. When the instruction word (module address, group address, and instruction) is stable on the REMOTE INPUT lines, the remote Instruction Transfer (INSTR) is inverted and applied to U11. The logic ZERO $\overline{\text{INSTR}}$ and $\overline{\text{REMOTE}}$ inputs enable U11 to decode the module address (MODAD 1 - MODAD 4) to activate one of the 16 output lines. (The proper module address is jumpered from one of the U11 output lines to E16.) When the module address is decoded, the logic ZERO output of U11 is delayed approximately 200 nanoseconds (in U5, R2, and C1) and then is output as the Input Request line (INRQ). Dropping INRQ to ZERO indicates to the remote programming device that the 720 has received the data. The U11 output is also routed to the group address decoder U6, where it is used as a strobe input.

U6 is a BCD-to-decimal decoder that determines (from the group address) which one of the five operating parameter instructions (Table 3-5) is being transmitted to the 720. The group address is decoded and one of the five output lines ($\overline{\text{STROBE 1}}$ through $\overline{\text{STROBE 5}}$) drops to logic ZERO when the output of U11 goes to a ZERO. Assuming that the group address to be decoded is 0 0 0 1 (group address for the MSD and 2nd SD of the bit rate parameter), the $\overline{\text{STROBE 1}}$ output drops to ZERO. The leading (negative-going) edge of this pulse clocks RMTIN 5 - RMTIN 8 into storage at U1. In the REMOTE mode, the A/B ENABLE input to U7 is at logic ZERO and the logic levels stored in U1 are coupled through U7 to the output lines. These output lines are the program control lines which are routed where required in the 720 to control the operating parameters.

At this point, it should be noted that the 720 can be programmed in the REMOTE mode; then switched to LOCAL mode and programmed by the front-panel switches and still retain the remote program in storage. Also, the program stored in the REMOTE mode may be modified by the front-panel OVERRIDE control. Depressing the OVERRIDE pushbutton raises $\overline{\text{REMOTE}}$ to a logic ONE. This input (A/B) to the input selection circuits of U1 connects the front-panel BIT RATE switch inputs (BR 1-1, -2, -4, and -8) to the storage latches in U1. Depressing the bit rate ENTER pushbutton drops $\overline{\text{ENTBR}}$ to a logic ZERO and the negative-going edge of this pulse clocks the manually selected bit rate into U1 stores. The MSD bit rate outputs from the U1 stores are routed through U7 to control the 720 program.

4.3.6 Format Store Card 8 (Figure 5-24)

Operation of the format store circuits is identical to that described for the bit rate store (paragraph 4.3.5). The operating parameters stored by these circuits are identified in the last three rows of Table 3-5. In the REMOTE mode, $\overline{\text{STROBE 3}}$ through $\overline{\text{STROBE 5}}$ (from group address decoder U6 on Bit Rate Store Card 7) clock corresponding parameters into storage.

4.3.7 DC Restorer Card 9 (Figures 4-9 and 5-26)

The circuits on this card perform two primary functions: DC restoration and bit decision. Each of these functions is described in the following paragraphs.

4.3.7.1 DC Restoration

The BIT DEC input from Filter Control Card 4 is applied to the positive inputs of comparators U32, U34, and U35. Assuming that filtered PCM is the 720 input, the F/S switch on the front panel is energized or the $\overline{\text{F/S}}$ command is loaded into Format Stores Card. The resulting logic ZERO $\overline{\text{BDF}}$ disables comparator U34, is inverted and applied as an enable input to AND-gates U37 which enable or disable comparators U32 and U35. The Q and $\overline{\text{Q}}$ outputs of bit decision flip-flop U2 determine which comparator is enabled. Assuming that the bit decision circuit has determined the current PCM bit to be a logic ONE, the logic ZERO $\overline{\text{Q}}$ output of U2 enables counter U21, U22 in the ONE's accumulator. The PEAK DEC input is compared with the ONE's accumulator (DAC) output at comparator U36. The output of U36 is clocked through flip-flop U2 to counter limits NAND-gates U25. The other inputs to NAND-gates U25 are from a decoder circuit that decodes the current count in U21, U22. If this count is at either limit, one of the decoder inputs to gates U25 prevents ONE's counter U21, U22 from counting in that direction. However, assuming the count stored in U21, U22 is within limits, the output of comparator U36 causes counter U21, U22 to count up or down, depending upon whether the analog voltage at the peak of the incoming bit was greater than, or less than, the value stored in the DAC. (The direction of the count is determined by the state of the up, down input. When low, the counter counts up and when high, the counter counts down.)

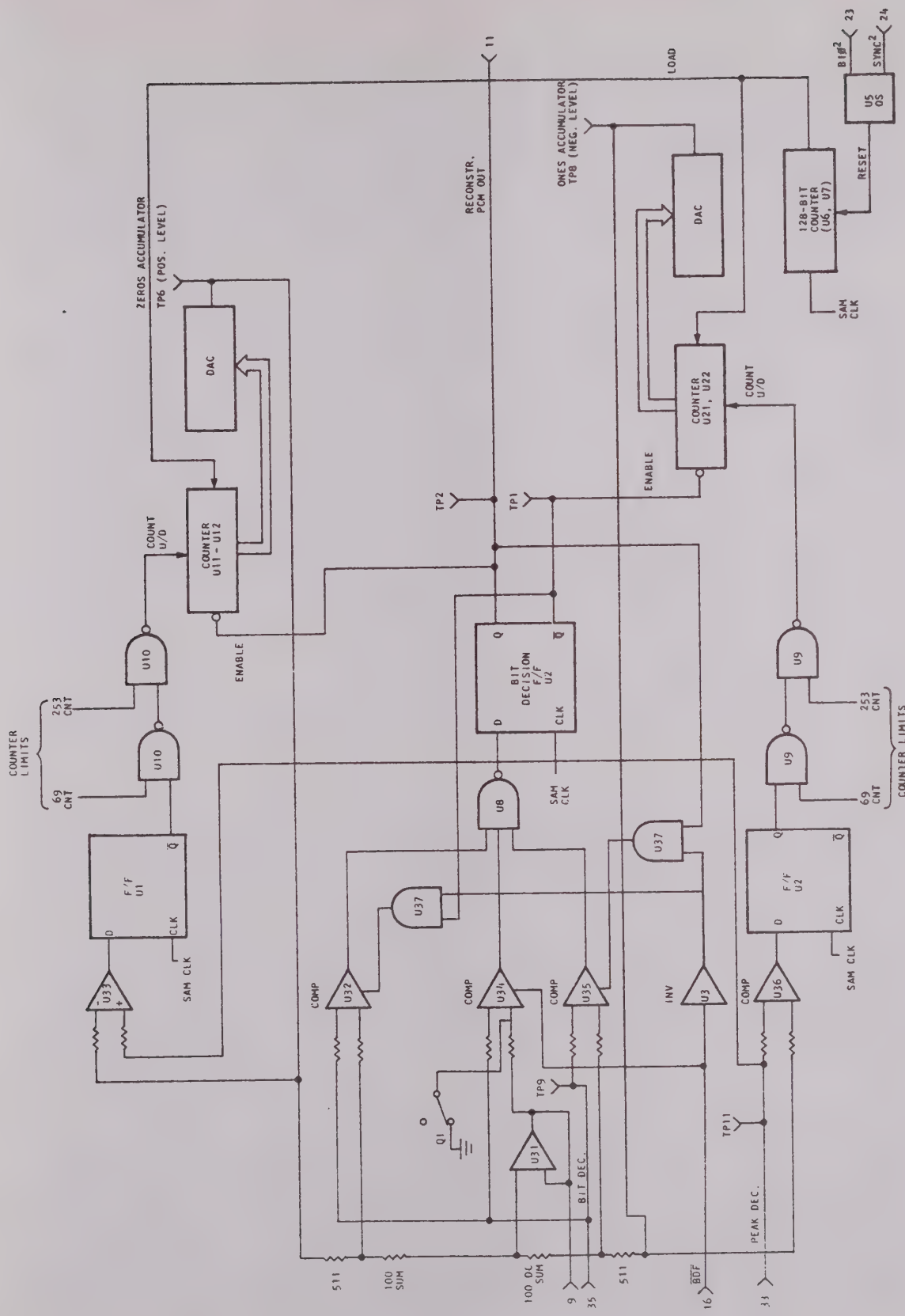


Figure 4-9. Simplified Schematic of DC Restorer

When the bit decision circuit determines that the incoming bit is a logic ZERO, the ZERO's accumulator circuit operation is identical to that described for the ONE's accumulator. Counter U11, U12 is enabled by the logic ZERO Q output of bit decision flip-flop U2. In this manner, the positive DAC continuously tracks the voltage value of the positive peaks of the PCM signal, while the negative DAC tracks the negative peaks. The two DAC outputs are summed to generate the PCM baseline and subtracted to generate the peak-to-peak signal level monitoring voltage.

The DC restorer contains a 128-bit counter (U4, U18) that is clocked by the internal sample clock (SAM CLK) and reset by a transition of either the Bi$\emptyset^2$ or SYNC^2 input from Loop Filter Card 5. If the counter is not reset before U6, U7 reaches a count of 128 (data dropout $\geq$ 128 bits), a LOAD output from U6, U7 enters a count of 253 (minimum voltage count) into both the ZERO's and ONE's accumulator counters. The 253 CNT output of the counter decoder circuits will then prevent either counter (ONE's accumulator U21, U22, or ZERO's accumulator U11, U12) from counting beyond this point. Resetting the counters in this manner causes the sum signal (which represents the PCM baseline) to return to zero whenever 128-bit periods occur without a transition being detected. This guarantees that the next zero-crossing of the PCM input will be detected as a transition. (If this were not done, the positive or negative DAC might lock up at maximum output and drive the sum signal to a level where no transitions are detected.)

The reconstructed PCM output of the DC restorer is taken from the Q output of bit decision flip-flop U2 and routed to the code converter circuits on card 10.

4.3.7.2 Bit Decision Circuit

The bit decision circuits consist of a voltage divider network, summing amplifier U31, comparators U32, U34, and U35, NAND-gate U8, and bit decision flip-flop U2. Operation of this circuit is discussed for NRZ, RZ, DM and Bi$\emptyset$ inputs.

As discussed briefly in paragraph 4.3.7.1, the operation of the bit decision circuit for NRZ codes depends on whether the square PCM (integrate and dump) mode or the filtered PCM (F/S) mode is selected. When the square PCM (I/D) mode is engaged, the $\overline{\text{BDF}}$ input (pin 16) is a logic ONE. This signal enables comparator U34 and disables comparators U32 and U35 by clamping their outputs to a logic ONE state. Under these conditions, the bit decision is made exactly as described later for RZ code.

When filtered PCM is selected, pin 16 is programmed to a logic ZERO state. This logic ZERO state holds the output of comparator U34 at a constant logic ONE. The incoming PCM NRZ is applied to the positive inputs of comparators U32 and U35. It should be noted at this point that the output of either U32 or U35 will be held to a constant logic ONE by a feedback input from bit decision flip-flop U2. If the preceding bit was a logic ONE, the output of U32 is held to a logic ONE level during the current bit decision by the logic ZERO on the $\overline{Q}$ output of U2. If the preceding bit was a logic ZERO, the output of U35 is held to a logic ONE by

PCM waveform varies depending upon the PCM code type being received by the 720. Paragraphs 4.3.8.1 through 4.3.8.9 describe code converter operation for each PCM code type.

4.3.8.1 Code Conversion with NRZ-L as the 720 Input

As shown in Figure 4-11, the reconstructed PCM input is already in NRZ-L form, delayed one bit time from the NRZ-L input to the 720. The internal clocks (CLK1 through CLK4) generated by VCO Card 6 are routed as inputs to and-or-invert (AOI) gate U8 in the clock selector circuit which consists of AOI gates U8-U9 and inverters U7. The remaining input to U8 is $\overline{Bi\emptyset\text{-}M + S}$ which is at a logic ONE level for all inputs codes except Bi$\emptyset$-M and Bi$\emptyset$-S. (When either of these codes is selected, $\overline{Bi\emptyset\text{-}M + S}$ drops to a logic ZERO.) With NRZ-L as the input code to the 720, CLK1 and CLK2 are passed through exclusive-OR U8 in their inverted form ($\overline{CLK1}$ and $\overline{CLK2}$). These signals are routed through inverters (U7) to generate the four output clocks as follows:

CLK1 becomes the 0° clock.

CLK2 becomes the 90° clock.

CLK3 becomes the 180° clock.

CLK4 becomes the 270° clock.

These clocks are routed to pins 16, 13, 15 and 14, respectively, of the card connector. The $\overline{CLK1}$ and $\overline{CLK2}$ outputs from U8 are also routed as follows:

a. $\overline{CLK1}$ is routed directly to pin 10 of one AND-gate in AOI gate U9B. $\overline{CLK1}$ is inverted and routed to the second AND-gate in U9B.

b. $\overline{CLK2}$ is routed as described in (a) above to the two AND-gates in exclusive-OR gate U9A.

Clock selection at AOI's U9A and U9B is controlled by the phase ($\emptyset$1 or $\emptyset$2) inputs from phase selector flip-flop U21B. With NRZ-L as the input code, flip-flop U21B is set and the logic ONE $\emptyset$1 output is routed to AOI's U9A and U9B in the clock selector logic. The resulting CLK1 output from U9B is routed through the sample clock selection logic (U11) as the sample clock (SAM CLK) output to DC Restorer Card 9. As shown in Figures 4-9 and 4-11, this signal samples the peaks of the filtered NRZ (FIL.NRZ) signal at the DC Restorer Card. The resulting reconstructed PCM output (RCNSTR. PCM) output from the DC Restorer is routed to the data input of delay flip-flop U20B and to U23A. Flip-flop U20B is not operable when the 720 is receiving NRZ-L inputs because the NRZ-L input to the set side of the flip-flop is at logic ZERO, holding the Q output at a logic ONE level. Also, with NRZ-L inputs and normal polarity selected at the 720 front panel, the POL output from U34C of the DC level logic is at a logic ZERO level. This signal causes U23A to function as a non-inverting buffer for the incoming reconstructed PCM. This signal is then applied to U23B

whose other input is the constant logic ONE Q output from U20B. The constant logic ONE Q output causes U23B to function as an inverter and the resulting DATA B output is gated to the data input of flip-flop U25B which synchronizes the NRZ-L output with the 0° clock. The NRZ-L output of U25B is routed to Output Driver Card 9 where it is amplified and inverted to normal polarity.

The preceding discussion assumed that normal polarity had been selected for the output NRZ-L code from the 720. If inverted polarity is programmed, the POL output from U34C in the DC level logic is a logic ONE level. This signal causes U23A to function as an inverter, and the additional inversion in the NRZ-L signal path causes the NRZ-L OUT from U25B to be of normal polarity. The additional signal inversion in Output Drivers Card 11 provides the desired inverted polarity.

4.3.8.2 Code Conversion with NRZ-M as the 720 Input

As shown in Figure 4-12, the reconstructed PCM input (pin 34) is delayed one bit time from the NRZ-M input to the 720. Internal clocks (CLK1 through CLK4) are received from VCO Card 6 and the four 720 output clocks (0°, 90°, 180°, and 270°) and the SAM CLK output to DC Restorer Card 9 are generated as described in paragraph 4.3.8.1. As with the NRZ-L code, the DC level generation logic routes a logic ZERO output (from OR-gate U33 which holds phase flip-flop U21B in a set condition. The logic ONE Ø1 output from U21B to the clock selector logic enables CLK1 to be routed to delay flip-flop U20B. With NRZ-M as the 720 input code, NRZ-L and BiØ-L connected to the set and reset sides of flip-flop U20B enables operation of the flip-flop by the clock (CL) and data (D) inputs. The reconstructed PCM is applied to the D input of U20B and to one input of U23A. Assuming that the normal polarity is programmed, the POL output of the DC level generation logic is a logic ONE for NRZ-M inputs to the 720. With POL at logic ONE, U23A functions as an inverter and the resulting wavetrain is applied to one input of exclusive-OR U23B. The reconstructed PCM is clocked into U20B by CLK1 and the DATA A (Q) output of U20B (delayed from the reconstructed PCM by one bit time) is exclusive-OR'ed in the U23B to generate the NRZ-L (DATA B) output. The spikes in the DATA B output are removed in output flip-flop U25 and the resulting NRZ-L OUT is routed to Output Drivers Card 11.

4.3.8.3 Code Conversion with NRZ-S as the 720 Input

Generation of the 0°, 90°, 180°, and 270° output clocks and SAM CLK to DC Restorer Card 9 is identical to that described in paragraph 4.3.8.1. As with NRZ-L and NRZ-M codes, the DC level generator holds the Ø1 output of U21B at a logic ONE level and this signal enables CLK1 as the clock input to delay flip-flop U20B. The reconstructed PCM is applied to the D input of U20B and to one input of U23A. With NRZ-S as the 720 input, the POL output from the DC level generator drops to logic ZERO, causing U23A to function as a non-inverting buffer of the reconstructed PCM input. This signal and the DATA A output of delay flip-flop U20B are exclusive-OR'ed in U23B to produce the DATA B output illustrated in Figure 4-12. The spikes in the DATA B output are removed in U25B and the resulting NRZ-L OUT is routed to Output Drivers Card 11.

4.3.8.4 Code Conversion with Biø-L as the 720 Input

With Biø-L as the 720 input, clock generation on the Code Converter is identical to that described for the NRZ inputs (refer to paragraph 4.3.8.1). The four output clocks (0°, 90°, 180°, 270°) are generated and ø1 selects CLK1 which generates SAM CLK for routing to the DC Restorer. SAM CLK strobes the reconstructed PCM from the DC Restorer and this wavetrain is routed to delay flip-flop U20B and to U23A. With Biø-L as the 720 input, the $\overline{\text{Biø-L}}$ input (from the DC level generator) to U20B drops to logic ZERO, effectively removing that flip-flop from the data path. With Biø-L as the 720 input and assuming that normal polarity is programmed, the POL output of the DC generator logic is at logic ZERO level and this signal causes U23A to function as a non-inverting buffer. The logic ZERO Q output of U20B also causes U23B to function as a buffer. The DATA B output of U23B is clocked through U25B and the resulting $\overline{\text{NRZ-L OUT}}$, delayed two bit periods from the Biø-L input to the 720, is routed to Output Drivers Card 11. Figure 4-13 illustrates Biø-L code conversion waveforms.

4.3.8.5 Code Conversion with Biø-M as the 720 Input

With Biø-M as the input code to the 720, the $\overline{\text{Biø-M + S}}$ output from the DC level generator drops to logic ZERO. This signal is routed to the clock selector logic where it enables the CLK3 and CLK4 inputs from VCO Card 6 to be gated through U8A and U8B. The outputs from these gates are routed through inverters to generate the output clocks as follows:

CLK3 becomes the 0° clock

CLK 4 becomes the 90° clock

CLK1 becomes the 180° clock

CLK2 becomes the 270° clock

However, the SAM CLK output to the bit decision flip-flop in DC Restorer Card 9, as in Biø-L, is still generated by CLK1. This clock remains the same because, in Biø-M, the logic ZERO output of U35A in the DC level generator resets U21B and the logic ONE ø2 output enables the CLK1 output of U9B in the clock selector logic. The reconstructed PCM is clocked (by SAM CLK) through the bit decision flip-flop on DC Restorer Card 9 to delay flip-flop U20B and U23A on the Code Converter Card. In Biø-M, the POL output of U34C in the DC level generator drops to a logic ZERO level causing U23A to function as a non-inverting buffer. The output of U23A and the Q (DATA A) output of delay flip-flop U20B are applied to exclusive-OR U23B. The resulting DATA B output is clocked with the 0° clock (CLK1) at output flip-flop U25B and the resulting $\overline{\text{NRZ-L OUT}}$ is routed to Output Drivers Card 11.

4.3.8.6 Code Conversion with Biø-S as the 720 Input

Generation of 0°, 90°, 180°, and 270° output clocks and the SAM CLK output (to DC Restorer Card 9) is identical to that described for Biø-M inputs in paragraph 4.3.8.5. Also, CLK1 remains the input clock to delay flip-flop U20B. However, with Biø-S as the 720 input, the POL output from U34C of the DC level

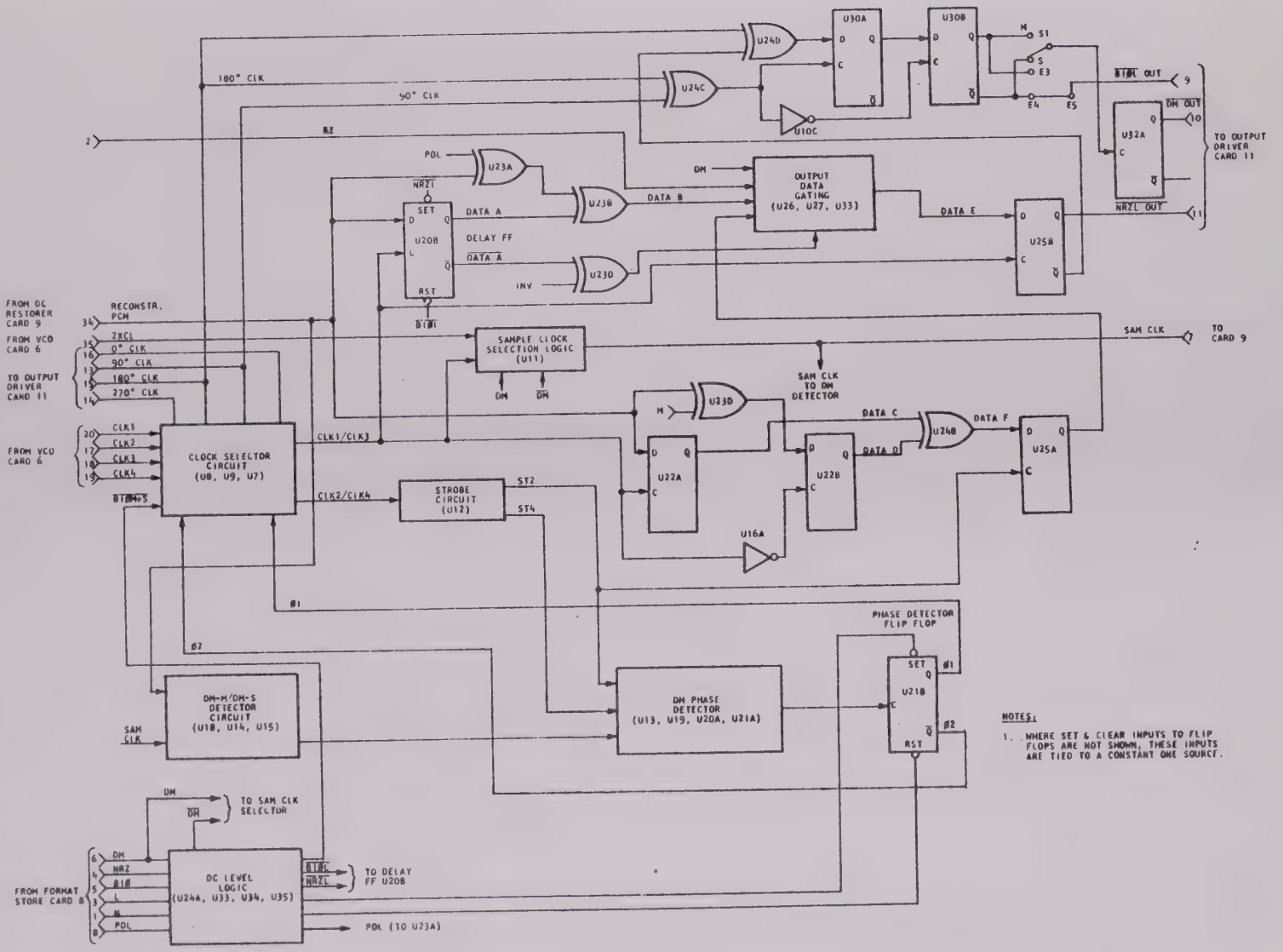


Figure 4-10. Simplified Schematic of Code Conversion Circuits on Card 10

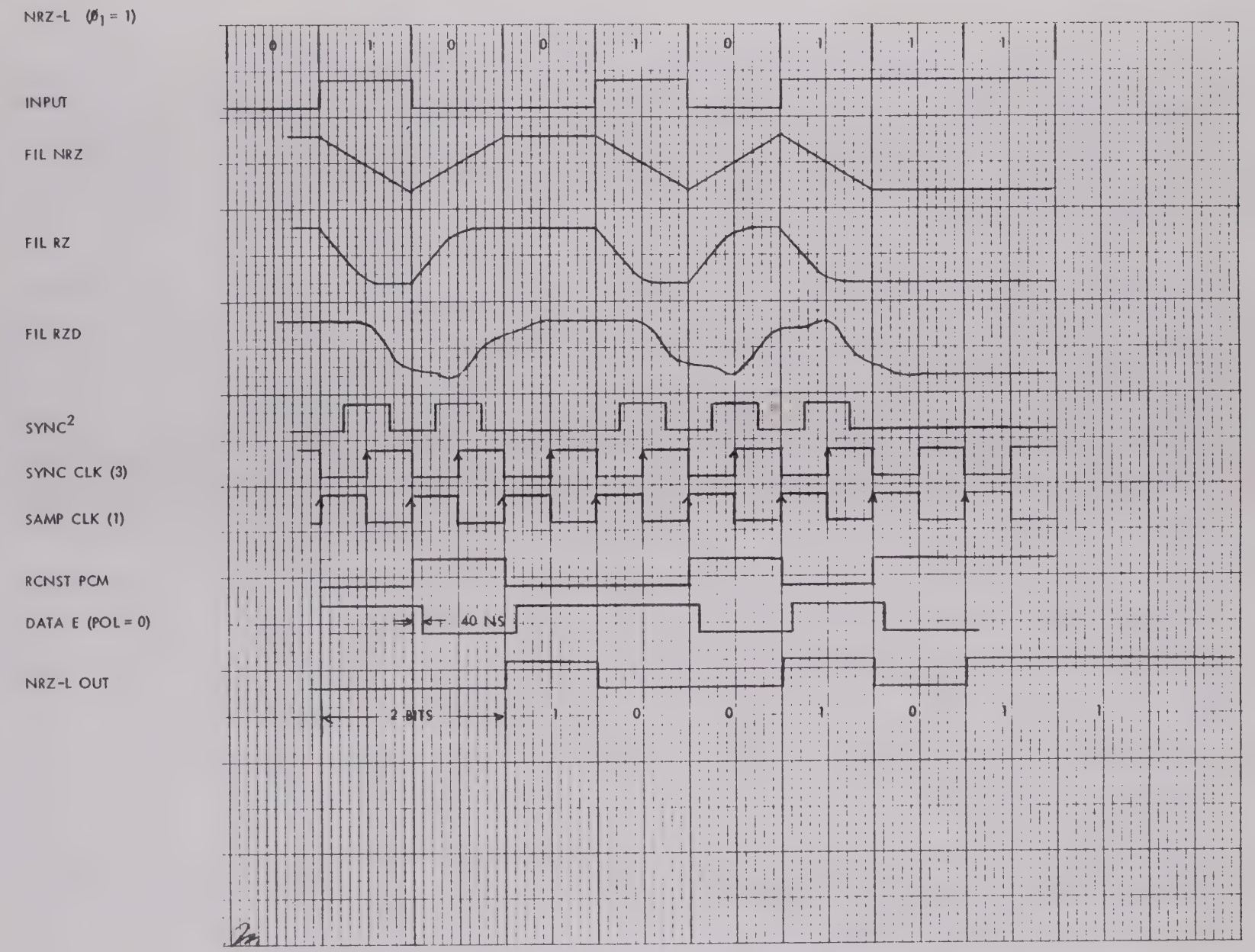


Figure 4-11. NRZ-L Code Conversion Waveforms

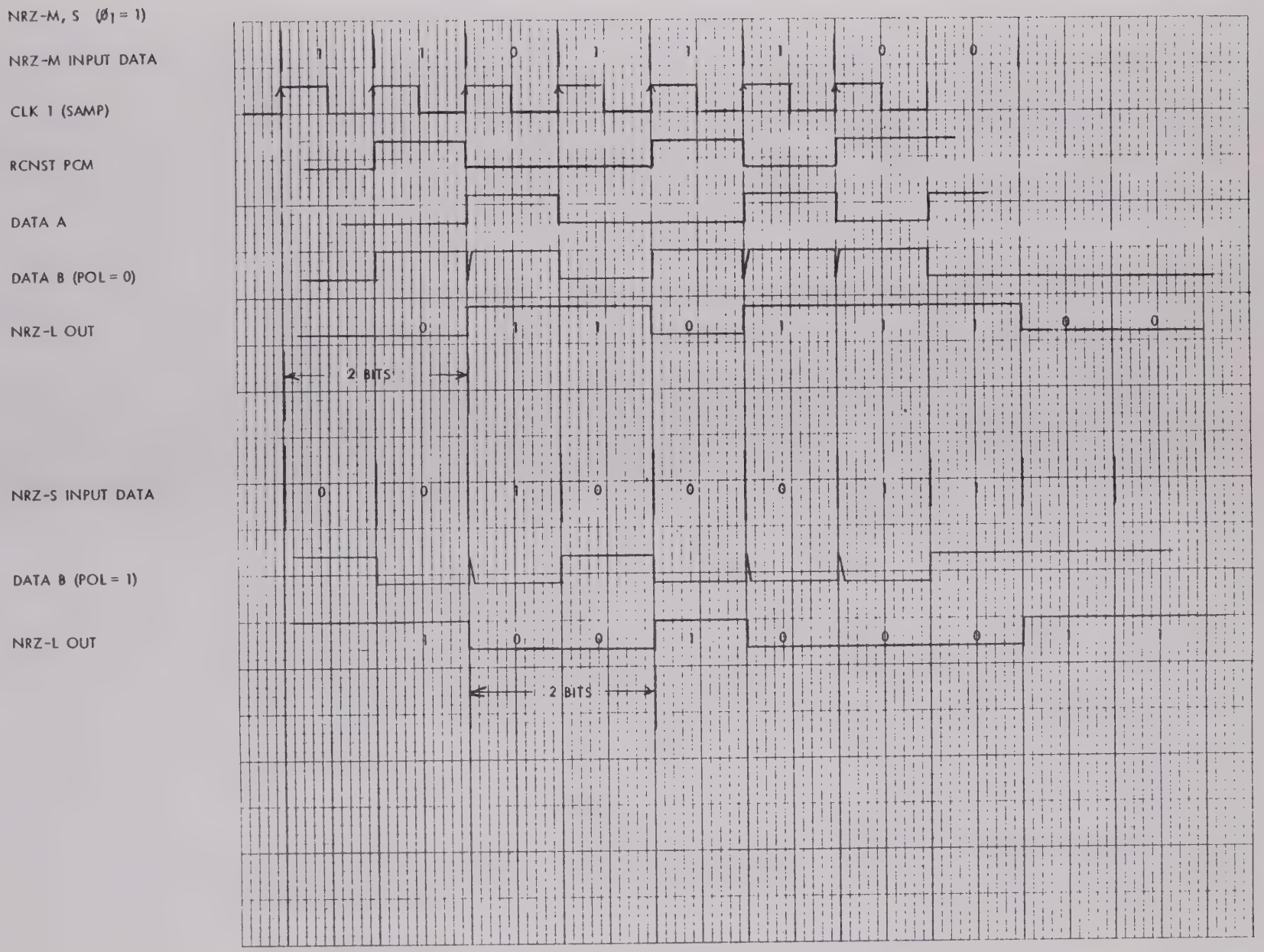


Figure 4-12. NRZ-M and S Code Conversion Waveforms

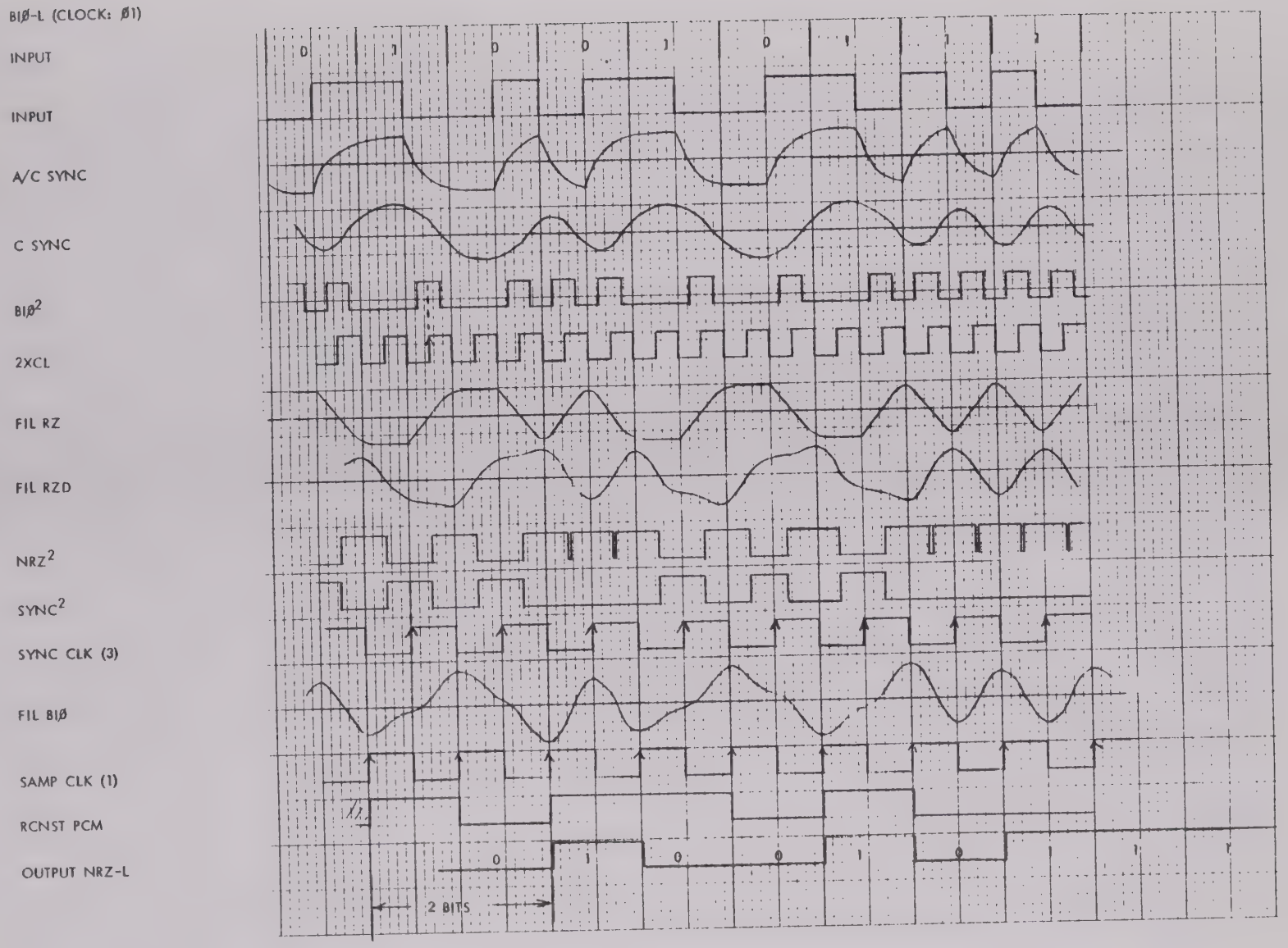


Figure 4-13. BiØ-L Code Conversion Waveforms

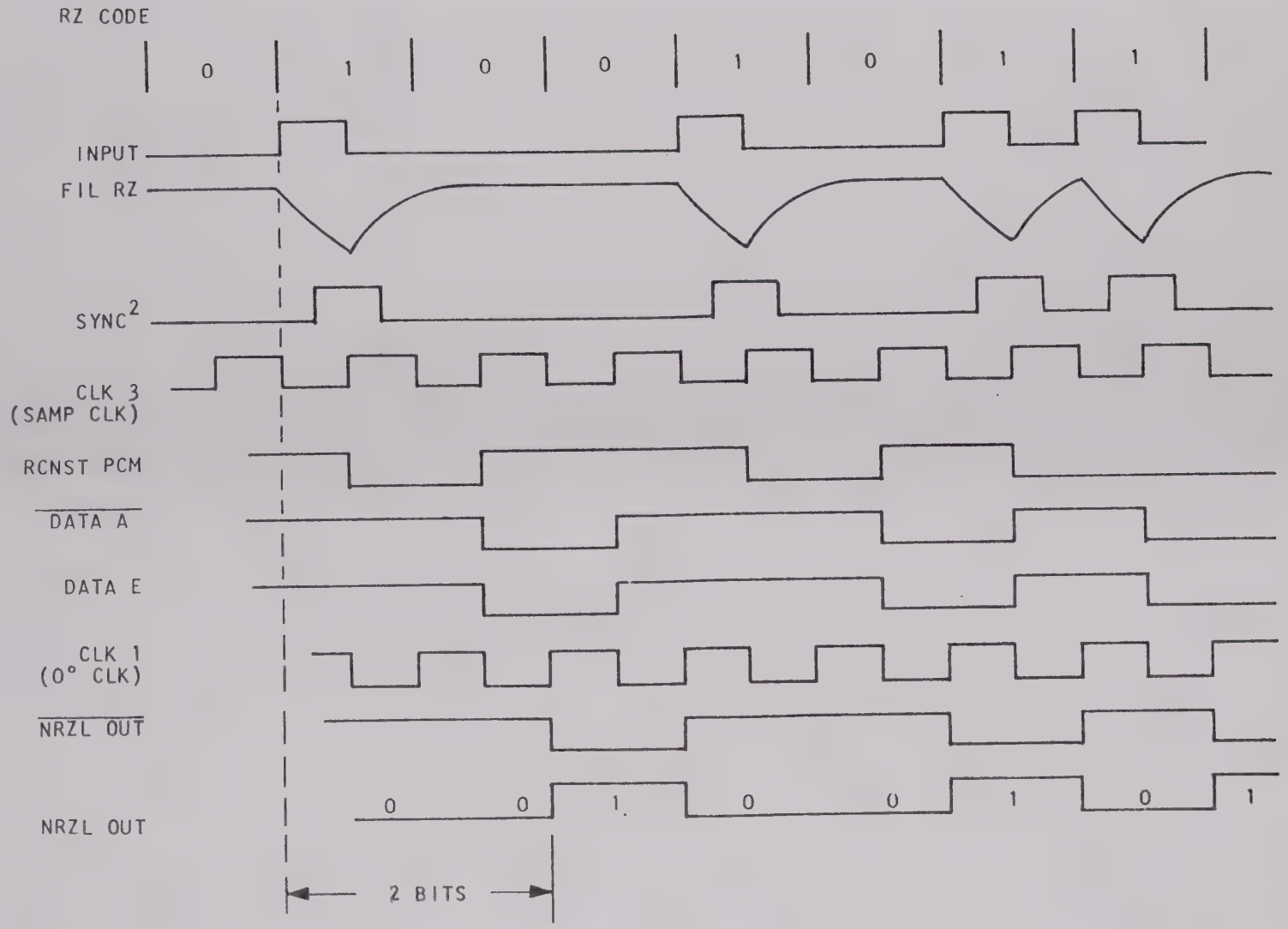
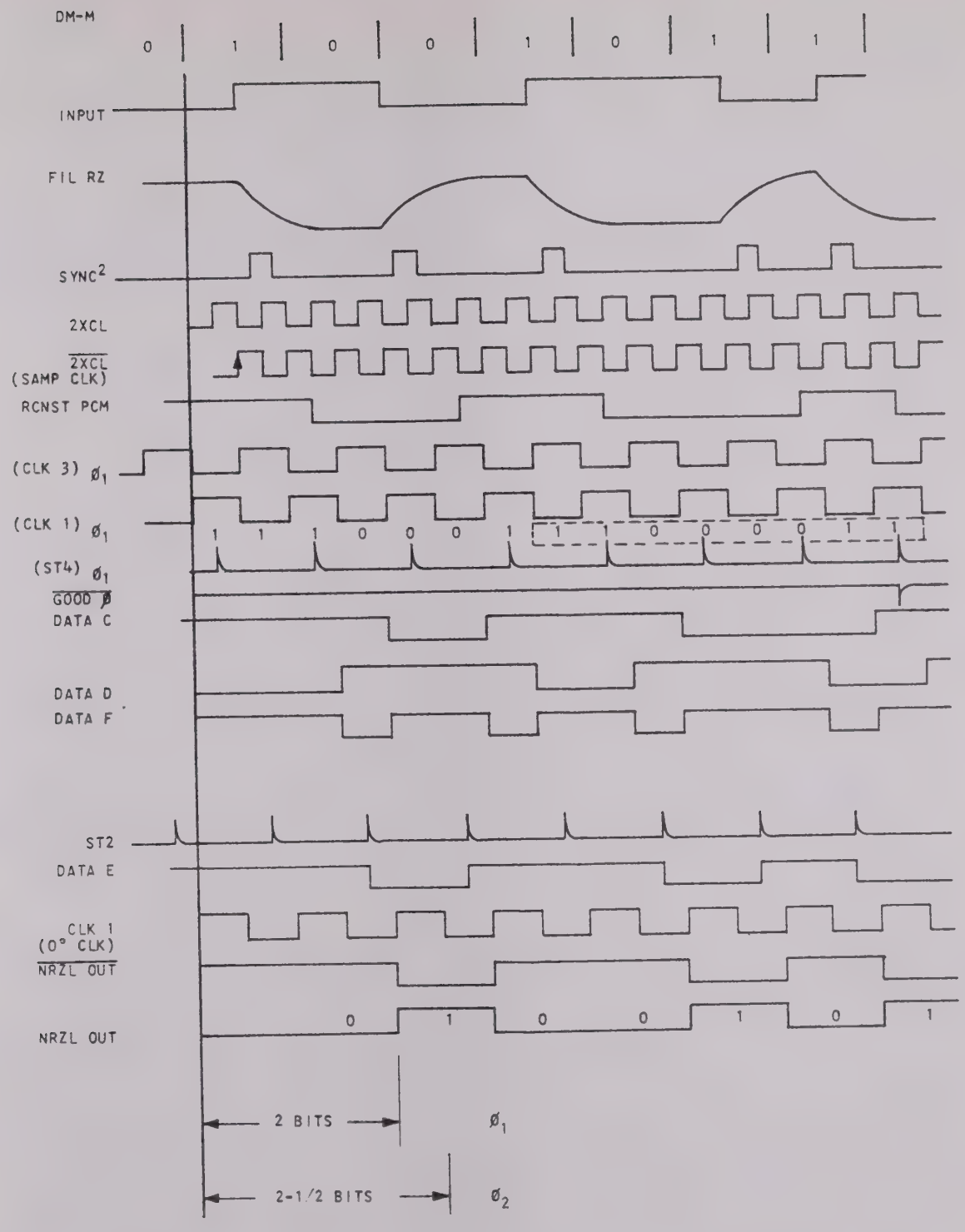


Figure 4-14. RZ Code Conversion Waveforms



NOTE: IF THE 720 LOCKS TO THE INPUT SIGNAL WITH THE ALTERNATE CLOCK PHASE, ALL WAVEFORMS BELOW THE RCNST PCM ARE DELAYED AN ADDITIONAL 1/2 BIT PERIOD (180°). UNDER THIS CONDITION, THE DM AMBIGUITY RESOLUTION CIRCUIT AUTOMATICALLY ENGAGES THE $Ø_2$ MODE.

Figure 4-15. DM Code Conversion Waveforms

generator is a logic ONE level and this signal causes U23A to function as an inverter. DATA B is clocked with the 0° clock (CLK1) in U25B and the resulting $\overline{\text{NRZ-L OUT}}$ is routed to Output Drivers Card 11.

4.3.8.7 Code Conversion with RZ as the 720 Input

With RZ as the 720 input, the CLK1 and CLK2 inputs from VCO Card 5 are gated through U8B and U8A, respectively, in the clock selector circuit. The outputs from these gates are routed through inverters to generate the output clocks as follows:

CLK1 becomes the 0° clock

CLK2 becomes the 90° clock

CLK3 becomes the 180° clock

CLK4 becomes the 270° clock

With RZ as the 720 input code (Figure 4-14), the output of NAND-gate U35A in the DC level generator drops to logic ZERO, and this signal resets phase flip-flop U21B. The logic ONE $\overline{Q}$ output (Ø2) of U21B enables CLK1 to be routed to U9B. The resulting CLK3 output is routed to delay flip-flop U20B and is also routed as the SAM CLK to the bit decision flip-flop in DC Restorer Card 9. The reconstructed PCM is clocked through the bit decision flip-flop by SAM CLK and is clocked through delay flip-flop U20B to U23D on the Code Converter Card. The other input to U23D provides inversion under control of the front-panel POLARITY switch, when the input RZ code is inverted. The output of U23D is applied to output data gating circuit U26. The resulting DATA E output is clocked with the 0° (CLK1) clock at output flip-flop U25B and $\overline{\text{NRZ-L OUT}}$ is routed to Output Drivers Card 11.

4.3.8.8 Code Conversion with DM as the 720 Input

With DM as the 720 input (Figure 4-15), the $\overline{\text{2XCL}}$ output from VCO Card 6 is inverted in gating circuit U11 and routed as the sample clock (SAM CLK) output to DC Restorer Card 9. This clock is also routed to shift register U18 in the DM detector circuit. The reconstructed PCM input from DC Restorer Card 9 is routed to the data input of shift register U18. The data is clocked into U18 by SAM CLK and the data pattern on the parallel output lines of U18 is decoded in NAND-gates U14 and U15. These decoder gates and their associated input inverters (U16 and U17) are configured so that a 00111100 output from U18 enables U14 and a 11000011 output from U18 enables U15. One of these patterns occurs whenever the DM-M code contains a 101 pattern or the DM-S code contains a 010 pattern. The outputs of U14 and U15 are OR'ed in U13C and the output of U13C is tied to the inputs of NAND-gates U13A and U13B. These gates are strobed by ST2 and ST4 which are derived from CLK2 and CLK4 in the clock selector circuit. When primary power is applied to the 720, the state of phase flip-flop U21B is undetermined and either the Ø1 or Ø2 output may be at a logic ONE level and phase status counter U19 is set to a count of 4. If Ø1 is high, CLK2 generates ST2 on its positive-going edge and ST4 on its negative-going edge. If Ø2 is high, CLK4 generates ST2 and ST4 the same way. The

selected clock (CLK2 or CLK4) is routed to the clock input of U20A. Assume that the data (D) input to U20A (from last stage of phase status counter U19) is a logic ZERO and the first clock input to U20A sets the $\overline{Q}$ output of U20A to logic ONE. This signal is routed as an enable input to "good phase" NAND-gate U13A. If the output of OR-gate U13C is high (logic ONE) when ST4 is generated, "good-phase" NAND-gate U13A is enabled and phase status counter U19 is clocked up by one count. If the output of OR-gate U13C is high when ST2 is generated, "bad-phase" NAND-gate U13B is enabled, causing phase status counter U19 to count down by one count. This process continues with U19 being clocked up or down, depending upon whether the output of U13C is high coincident with ST2 or ST4. Whenever U19 reaches a count of 8, the logic ONE output from U19 is clocked into U20A by CLK2 or CLK4. The resulting logic ZERO $\overline{Q}$ output from U20A disables U13A, preventing further "count-up" pulses from entering U19. However, U13B will still provide "count-down" pulses whenever the output of U13C is high coincident with ST2. The first count-down input to U19 will reduce the count to 7, removing the logic ONE from the D input of U20A. The next (CLK2 or CLK4) pulse changes the state of U20A, enabling count-up gate U13A. If the reconstructed PCM is out of phase, the count-down process of U19 continues until a count of zero is reached. At this time, a logic ZERO BORROW output is inverted and used to clock phase flip-flop U21B. The resulting logic ONE Ø2 line to the clock selector logic (1) enables CLK3 inputs to DM comparison flip-flops U22A and U22B, and (2) enables CLK2 inputs to the ST2 and ST4 strobe generation circuits. The logic ZERO BORROW output of U19 clears (counter) load control flip-flop U21 and the logic ZERO load (LD) input to U19 enables a preset count of 4 to be entered into U19.

The count-up/count-down process continues and, if a phase correction is made, the count-down procedure described above will change the state of phase flip-flop U21B and the Ø1 input to the clock selector logic will rise to a logic ONE level, enabling CLK1 to drive the DM comparison flip-flops (U22A, U22B) and enabling the CLK4 inputs to ST2 and ST4 strobe generation circuits. The reconstructed PCM input at pin 34 is routed to the data input of flip-flop U22A and to one input of U23D which functions (1) as an inverter if DM-M is the 720 input code, or (2) as a non-inverting buffer if DM-S is selected. U22A, U22B, and exclusive-OR U24B function as a comparison circuit that compares the data in the first half of every bit period with the data in the second half of the bit period. This comparison detects the DM code, for the difference between 1's and 0's in the DM code is the transition at mid-bit period. For DM-M, the mid-bit transition represents a 1; for DM-S, a zero. By inverting the reconstructed PCM in U23D for DM-M code, the output of U24B is required to be a 1 whenever the selected DM code represents a 1. The output of U24B is clocked through U25A by ST2 which may be in phase (Ø1 selects CLK4 in clock selection circuit) or may be 180° out of phase (Ø2 selects CLK2 in clock selection circuit). The resulting output is routed through NAND-gate U26C and OR-gate U27A to the data input of code converter output flip-flop U25B. At this point, the data is clocked with the 0° clock and the resulting inverted $\overline{\text{NRZ-L OUT}}$ is routed to Output Drivers Card 10. It should be pointed out that the DM code ambiguity results in a 1/2 bit uncertainty in the bit delay of DM codes from input to output of the 720. When the ambiguity resolution circuit detects the correct phase, it

does so by slipping the output data by a half bit rather than switching clock phases. Consequently, the bit delay of the 720 for DM codes may be 2 or 2-1/2 bits, while for all other codes it is 2 bits.

4.3.8.9 DM and Biø-L Tape Outputs

For all 720 input codes, a code conversion circuit [consisting of (1) exclusive-OR gates U24C and U24D, (2) flip-flops U30A and U30B, (3) card-mounted DM code selector switch S1, and (4) DM output flip-flop U32A] provides Biø-L and DM outputs suitable for tape recording. The NRZ-L output of U25B and the 180° clock are applied to exclusive-OR U24D. The resulting Biø-L output is routed to the D input of U30A. The 180° clock and the 90° clock are applied to exclusive-OR U24C to generate 2XCL which is used as the clock input to U30A. The $\overline{\text{2XCL}}$ output of inverter U10C is used as the clock input to U30B. Flip-flop U30A removes the spikes from the Biø-L input from U24D and U30B generates a 1/2 bit time delay so that the $\overline{\text{Biø-L}}$ and NRZ-L OUT (from Q of U25B) are in phase. Card-mounted toggle switch S1 enables selection of Biø-L or $\overline{\text{Biø-L}}$ as the clock input to DM flip-flop U32A. When S1 is set to position M, Biø-L output of U30B is selected as the U32A clock and $\overline{\text{DM-M}}$ is the output code at pin 10. When S1 is set to position S, $\overline{\text{Biø-L}}$ is selected as the U32A clock and $\overline{\text{DM-S}}$ is the output code at pin 10. The $\overline{\text{Biø-L}}$ and $\overline{\text{DM}}$ outputs are routed to Output Drivers Card 10.

4.3.8.10 Sync Detector Circuit

The function of the sync detector circuit is to determine whether or not the 720 is phase locked with the incoming PCM signal. This is accomplished by comparing each pulse in the SYNC^2 signal for coincidence with both the correct and incorrect phase of the 720's internally generated clocks. The ratio of correct coincidence to incorrect coincidence is averaged in an RC integrator, and a decision is made by a threshold comparator. This technique tends to average the effects of noise and transition density, and provides a reliable SYNC indication down to a SNR of 3 dB with random data (NRZ and Biø codes). The circuit consists of clock selectors U1A, U1B, a strobe generator (U2C, U2B, U1C, U2A), strobe gates U1D and U3B, phase detector flip-flop (U3D, U3C) and comparator amplifier U5. For all 720 input codes (except DM-M and DM-S), the CLK1 input is gated through U1B to the strobe generator. This circuit generates a strobe at the leading and trailing edge of each clock input. The outputs from the strobe generator are applied to NAND-gates U1D and U3B. The SYNC^2 input from Loop Filter Card 5 is the second input to both gates. (If the SYNC^2 input is in phase with the leading edge of CLK1, U1D is enabled and the negative-going strobe output sets cross-coupled flip-flop U3D-U3C.) The logic ONE output of U3D is filtered, integrated into a DC level, and applied to U5 for comparison with the threshold level which is set (by R16) at approximately 75% of the DC level derived from the U3D output. The output of U5 is AND'ed with $\overline{\text{ZERO SIG}}$ from Loop Filter Card 5 and the output of 0.5 sec one-shot U6. When the three inputs to U4A are at logic ONE levels, a logic ONE (LOCLITE) output turns on the front-panel SYNC lamp. If input signal to the 720 is lost, ZERO SIG drops to logic ZERO and the resulting logic ZERO output from U4A turns off the SYNC lamp. Similarly, if the $\overline{\text{128 CTR}}$ input drops to ZERO, indicating

that 128 consecutive bit periods have passed without a transition, one-shot U6 is fired and the SYNC lamp is turned off for 0.5 second. If the SYNC^2 input is in phase with the trailing edge of CLK1, U3B is enabled and the negative-going strobe output resets the cross-coupled flip-flop. The output of U3D drops to logic ZERO, causing the output of comparator U5 to drop to ZERO. AND-gate U4A is disabled and the LOCLITE output drops to logic ZERO, turning off the SYNC lamp.

4.3.8.11 UBE and LBE Detector Circuits

The deviation status (DEV ST) input from Loop Filter Card 5 is a signal that represents any frequency deviation of the 720 input from the selected bit rate. This signal is applied to the UBE detector (U29, U36B, and U31A) and the LBE detector (U28, U36A, and U31C). The UBE and LBE detector circuits determine when the 720 input exceeds ±70% of the tracking range and transmit a 5-volt (LBE or UBE) output to rear-panel connector J2 when either condition exists.

4.3.9 Output Drivers Card 11 (Figure 5-30)

The output buffer amplifiers for the NRZ-L output and the four clock outputs are identical, and consist of a complementary transistor pair in an emitter-follower configuration. The output buffer is virtually a voltage source (very low impedance) up to the point where current limiting occurs. The output supply (ONE level) current is limited to 50 mA and, consequently, is short-to-ground protected. The output sink (ZERO level) current is not limited and, consequently, shorting the output to a supply voltage may damage the output circuitry. The low impedance output characteristics of the buffer circuits require that any output cable more than a few feet long must be terminated in its characteristic impedance. The output voltage levels are standard TTL levels.

The tape output (BiØ-L and DM) buffer circuits differ from the others in that a Zener diode is used to offset the TTL level signals to make them bipolar. In addition, resistors in the emitter circuits of the output transistors increase the output impedance to approximately 65 ohms. Each circuit is designed to output a 2-volt peak-to-peak signal, centered about ground, into a 50-ohm, terminated cable.

4.3.10 Power Supply and Regulator Card 13 (Figures 5-2 and 5-32)

The power supply and regulator circuits operate from a primary AC power input to generate the DC voltages necessary for bit synchronizer operation. These circuits are contained on the bit synchronizer Right Side Panel Assembly A3 and on the Regulator Card, located at connector J13 of Interconnection Assembly A1. The power supply circuit is illustrated in Figure 5-2, wiring diagram for the bit synchronizer, and the voltage regulator schematic is Figure 5-32. Interconnections between the power supply and voltage regulator are illustrated in Figure 5-4, schematic diagram for Interconnection Assembly A1.

As shown in the above figures, the primary AC power is applied via POWER switch A3S1 to the primary winding of power supply transformer A3T1. Two secondary windings of A3T1 apply reduced AC voltage (nominally 26V AC) to supply the ±18V regulators on the Regulator Card. The 15V AC output of the remaining secondary winding is full-wave rectified at A3CR1 and then applied to the Regulator Card to supply the +5V regulator. The Regulator Card contains three regulator circuits: a +18V regulator, a −18V regulator, and a +5V regulator. The 26V AC inputs from A3T1 are applied to full-wave bridge rectifiers CR1-CR4 and CR5-CR8. The unregulated DC outputs of these rectifiers are applied to voltage regulator microcircuits U1 and U3, respectively. The unregulated DC output of A3CR1 is routed to voltage-regulator microcircuit U2. Each voltage regulator consists of a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and current limit circuitry. Regulation (in each regulator) is accomplished by comparing the output of the regulator with a voltage reference obtained from a Zener diode. A differential amplifier senses the magnitude and direction of a voltage difference from the reference and regulates the biasing of the series control.

Current supplied at the regulator output is limited by a current limiting stage. This stage samples voltage developed across a series resistance and, if this voltage is sufficiently high, reduces the biasing of the series control. All regulators are current limited and short-circuit protected.

MAINTENANCE

SECTION 5

MAINTENANCE

5.1 GENERAL

This section contains information to aid in troubleshooting and maintaining the Model 720 Bit Synchronizer. This information is intended for use with the theory of operation, contained in Section 4, so that maintenance may be performed with maximum efficiency. Included in the maintenance information are troubleshooting guides (paragraph 5.2), wiring (paragraph 5.3), and assembly and schematic diagrams for all bit synchronizer subassemblies (Figures 5-1 through 5-32).

5.2 TROUBLESHOOTING

In the event an abnormal condition is detected in bit synchronizer operation, the following general method of isolating and repairing the trouble is recommended:

a. Perform visual inspection (paragraph 5.2.1).

b. Perform test and adjustment procedure to isolate the malfunctioning circuit (paragraph 5.2.2).

c. Malfunctioning component is isolated by using the printed-circuit card data in Section 4, and the schematic and assembly diagrams (Figures 5-1 through 5-32).

d. When defective component is located, refer to Section 6, Parts Lists, for replacement component information.

e. Perform test and adjustment procedure to ensure that malfunction is corrected (paragraph 5.2.2).

5.2.1 Visual Inspection

The bit synchronizer should be subjected to a regular inspection program similar to that recommended for other types of electronic equipment. The following inspection should be performed periodically as a means of preventive maintenance or, if a malfunction occurs, to aid in isolating the trouble.

a. Inspect front- and rear-panel components for signs of damage.

b. Inspect printed-circuit cards and mating connectors for mechanical damage or component discoloration.

c. Inspect wiring for loose or broken connections.

5.2.2 Test and Adjustment Procedure

Once the 720 has been initially tested and adjusted, no periodic adjustments are required unless a malfunction occurs. This procedure is intended as an aid in determining whether or not the unit is operating normally and, if not, to assist in isolating the problem. Before any adjustments are performed on the 720, a minimum warmup period of 15 minutes should be allowed.

The test and adjustment procedure is divided into three main sections. The first section provides a list of test equipment required. The second and third sections outline the steps in checking and adjusting the power supply-regulator circuits and the bit synchronizer circuits, respectively.

5.2.2.1 Test Equipment Required

1 50 MHz Oscilloscope

1 PCM Signal Simulator

1 HP 3459A DVM or equivalent

1 Frequency Counter, accurate to ± 0.1% or better

1 Elgenco 610A Noise Generator or equivalent

1 Sine-Wave Generator

5.2.2.2 Power Supply and Regulator Circuits

CAUTION

Do not apply power to the regulator card with open circuits across terminals E1 and E2, E3 and E4, or E5 and E6.

a. Using a DVM, check the regulated DC voltages at the appropriate test points on the Regulator Card 12 as follows:

TP4 -- +5.00V ± 1%

TP1 -- +18.00V ± 1%

TP3 -- −18.00V ± 1%

b. If the outputs in step (a) above are not as stated, the +5V, +18V, and −18V regulated output voltages are adjusted by test variables R21, R7, and R8, respectively.

5.2.2.3 Source Selector and Input Amplifier Card 1

a. Using a PCM signal simulator, apply a PCM signal to one of the input connectors. Select LOCAL programming and program the 720 appropriately for the input signal utilized.

b. On the 720 front panel, monitor the INPUT test point. The signal shall be a duplication of the input PCM signal, possibly altered in amplitude, but in no other way. Check at both low (10 kbps) and high (2 to 5 Mbps) bit rates.

c. If the PCM signal at the INPUT test point varies from step (b) above, adjust C14 on card 1. High frequency compensation of the input attenuator is provided by this capacitor, which should be adjusted to minimize distortion of the signal at the INPUT test point with a square-sided, PCM input of 10 kbps (low bit rate). (This adjustment is similar to adjusting the rise time of a scope probe.)

5.2.2.4 Input Filter

The operation of the input filter can be checked by observing the signal waveforms on the Filter Control Card 4. Figure 5-33 shows the input and output signals at the appropriate test points for proper operation of the input filter for the NRZL, BiØL, and RZ codes. It should be pointed out that some distortion (i.e., overshoot) of the signals shown occurs at bit rates above 1 Mbps

The synchronization outputs ($SYNC^2$ and $Bi\emptyset^2$) of the input filter can be checked out by observing the logic level signals at TP1 and TP2 as follows:

a. Apply an NRZL PCM signal to the 720 and program the unit accordingly. The signal at TP1 shall be a 1/2 bit period pulse shortly following each transition of the input PCM signal.

b. Apply a BiØL PCM signal and program the 720 accordingly. The signal at TP2 shall be a 1/4 bit period pulse shortly following each transition of the input PCM signal.

c. Apply an RZ PCM signal and program the 720 accordingly. The signal at TP1 should be a delayed regeneration of the input PCM signal.

5.2.2.5 Phase-Locked Loop

Operation of the phase-lock loop is dependent on VCO Card 6 and Loop Filter Card 5. A quick operational test to see that the loop is locked to the incoming signal can be made by monitoring TP4 on card 5. For NRZ codes, and for bit rates below 1 Mbps, the signal at this point should be a tri-level pulse train, as shown in Figure 5-34. A single tri-level pulse is generated by each transition in the input PCM signal. For BiØ codes, the tri-level pulse train contains pulses of amplitudes and pulse lengths as shown in Figure 5-35. At bit rates above 1 Mbps, the pulses become increasingly averaged by the response time of the amplifiers and, consequently, become distorted. However, the loop still responds to the averaged signal.

5.2.2.6 VCO Card Calibration

There are three potentiometers on the VCO Card to facilitate adjustment of the center frequency, modulation gain, and symmetry of the two-times clock (2XCL) output. No adjustment of these controls should be necessary unless a malfunction has occurred and repairs have been made to the VCO Card.

To calibrate the VCO Card, it is necessary to set up the card in a test jig or on an Extender Card with the connection to pin 24 broken out. Adjustments are made as follows:

a. Center Frequency Adjustment: Ground pin 24 and adjust R58 until the selected bit rate ± .05% is generated. Measure the bit rate by connecting a counter to one of the clock outputs of the 720. For this test, a bit rate below 1 Mbps should be selected.

b. Modulation Gain Adjustment: Inject a 3 Hz, 3V peak-to-peak sine wave, centered about ground, at pin 24. Monitor TP7 with an oscilloscope, and adjust R57 for minimum perturbation.

c. Symmetry Adjustment: R72 adjusts the symmetry of the two times clock (2XCL) signal. This potentiometer should be adjusted under the loop filter alignment procedure (paragraph 5.2.2.7). However, if the VCO refuses to oscillate, R72 may be at fault and should be adjusted to its mid-point by counting turns. Whenever R72 is adjusted, a re-alignment of the loop filter should be performed.

d. Recheck the center frequency and readjust R58 if necessary (pin 24 grounded).

5.2.2.7 Loop Filter Alignment

There are 5 pots on the loop filter to facilitate balancing the loop to optimize acquisition and sync threshold performance. A rough calibration can be carried out with a minimum of test equipment as follows (Note: Allow 15 minutes warm-up before performing this calibration):

1. DC Balance: With 720 input grounded, adjust R100 to zero the DEVIATION meter in the 0.1% loop width.

2. Noise Balance: Connect an Elgenco 610A noise generator to the 720 input. Program the unit and adjust the 610A as shown in the table below for each adjustment. Set sufficient noise amplitude to keep SIG LOSS lamp out. Adjust for best zero of the DEVIATION meter over all bit rates and codes in the 0.1% loop width.

Adjustment	Noise Bandwidth	Bit Rate	Code
Low Frequency NRZ (R102)	2 MHz	500 kbps	NRZ-L
High Frequency NRZ (R89)	5 MHz	3.9 Mbps	NRZ-L
Low Frequency BiØ (R106)	2 MHz	500 kbps	BiØ-L
High Frequency DM (R109)	5 MHz	2.5 Mbps	DM-M

5.2.2.8 Sync Indicator Adjustment (Code Converter, Card 10)

Adjustment of the sync indicator circuit requires the generation of a test PCM signal with a precise SNR. With a 3 dB SNR, random data, NRZ code and 0.1% loop width, adjust R16 on the Code Converter card until the green SYNC lamp just illuminates. This should be carried out at a bit rate of 2.5 mB.

5.3 WIRING

The bit synchronizer wiring information is contained (1) in the 720-02 wiring diagram (Figure 5-2), (2) the interconnection board (A1) wiring diagram (Figure 5-4), (3) the front subpanel assembly (A2) schematic (Figure 5-6), and (4) the individual card schematics also contained in this section. Input/output signal identification is furnished in Tables 3-1 through 3-4 of Section 3.

As shown in Figure 5-1, Front Subpanel Assembly A2 plugs into connector J14 on Interconnect Assembly A1. Signal tracing between circuits on Front Subpanel Assembly A2 and the card assemblies and switches on Interconnect Assembly A1 is facilitated using the associated schematics on Figures 5-6 and 5-4, respectively. The only connections between Assemblies A1 and A2 that are not routed through connector J14 (on A1) are the connections to Assembly A2 test points TP2 (NRZ-L OUT) and TP3 (0° CLOCK). These connections are made directly from the terminals (E62, E64) on Assembly A1 to the test points (TP3, TP2) on Assembly A2 as illustrated in both Figures 5-2 and 5-6. On the 720-02 wiring diagram (Figure 5-2), four 14-pin connectors (A4J23 through A4J26) are shown. These connectors plug into mating connectors (A1J7P2, A1J7P3, A1J8P2, A1J8P3) mounted on the respective card assemblies. Signal tracing is performed using the individual card schematics and the 720-02 wiring diagram (Figure 5-2).

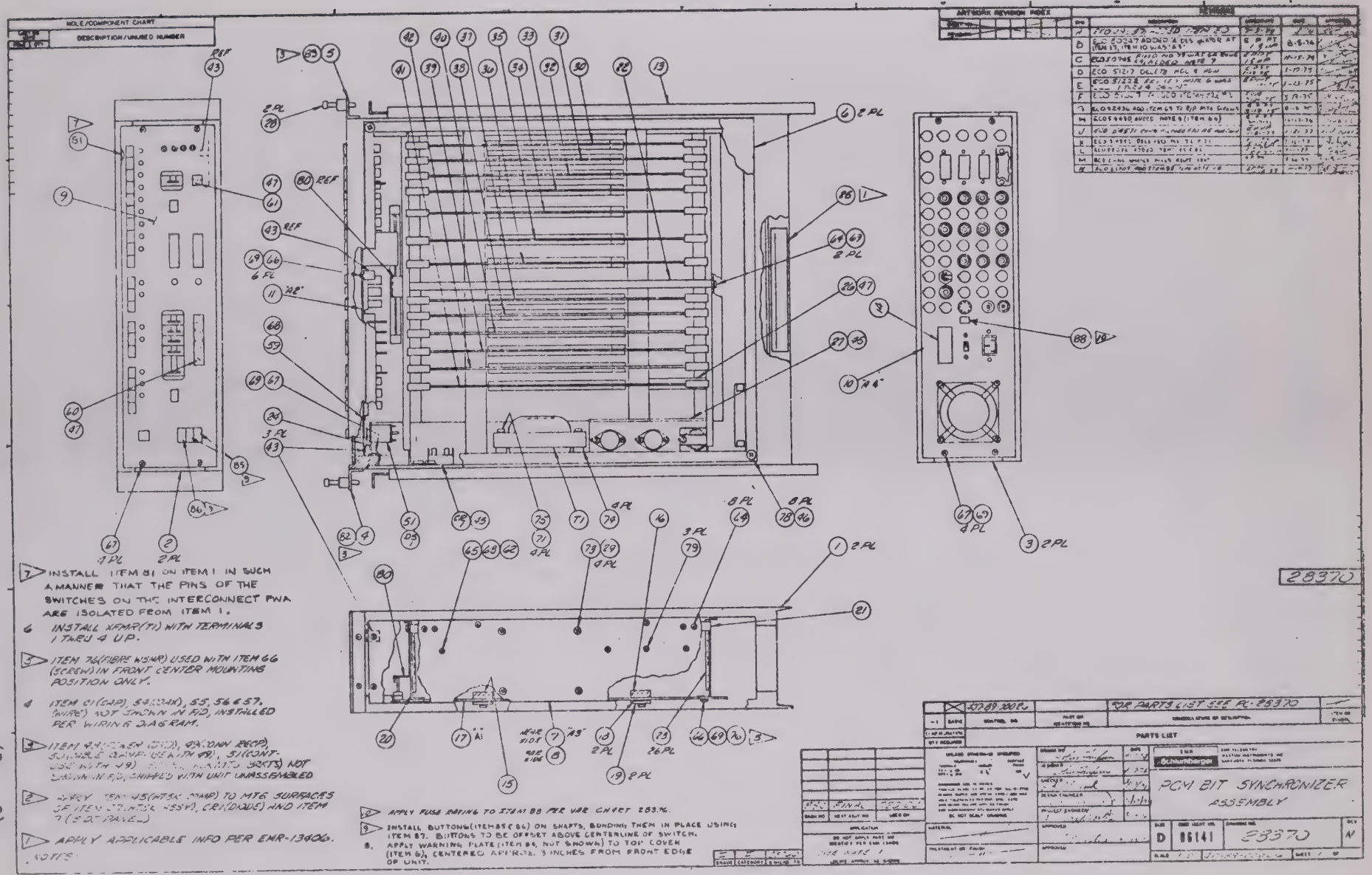
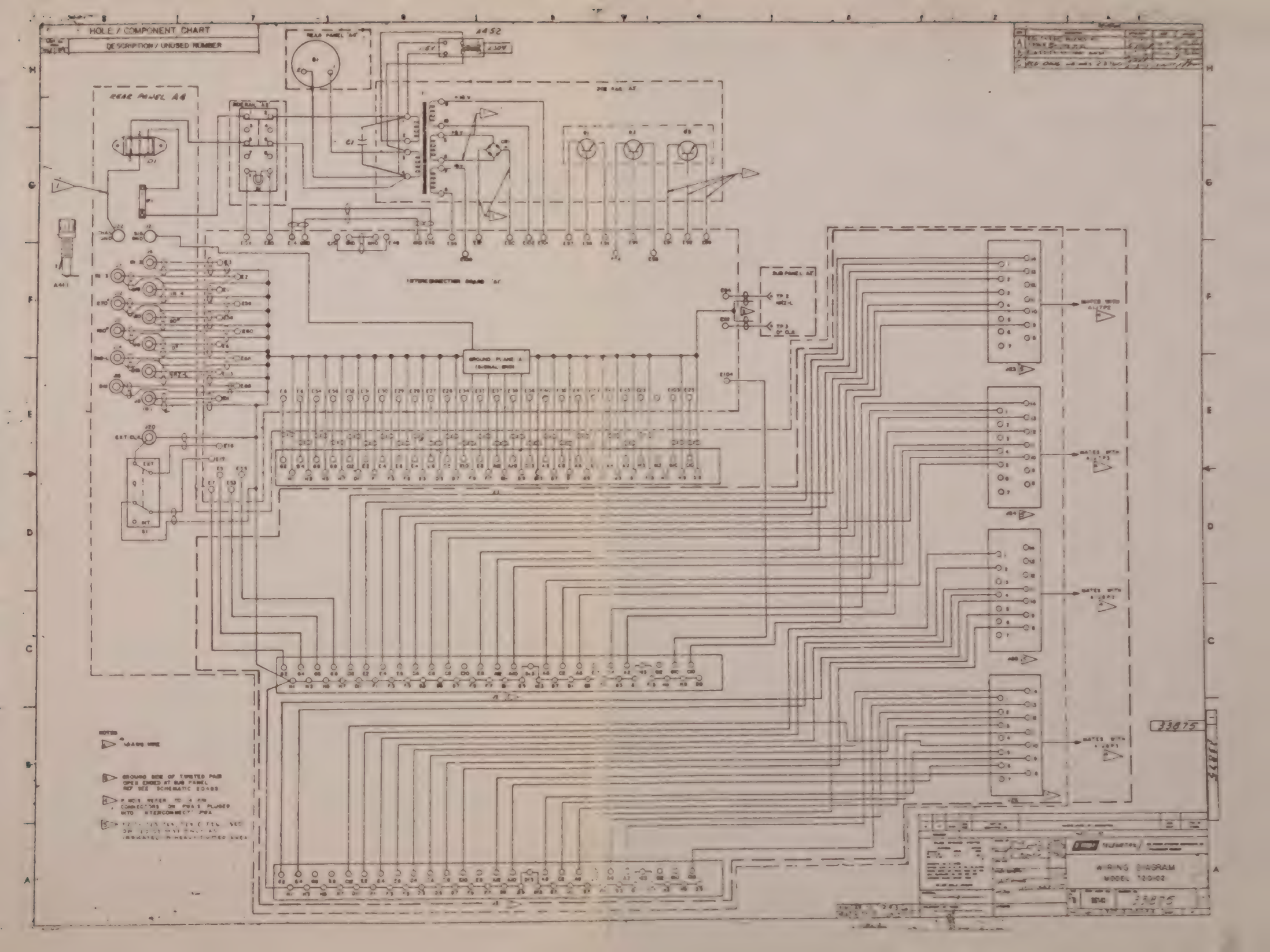


Figure 5-1. Model 720-02 Bit Synchronizer Assembly Diagram


HOLE / COMPONENT CHART
DESCRIPTION / UNUSED NUMBER
REAR PANEL A4
A452
INTERCONNECTION BOARD 'A'
GROUND PLANE A
SUB PANEL A2
EXT CLK
EXT
INT
33875
WIRING DIAGRAM
MODEL 720102

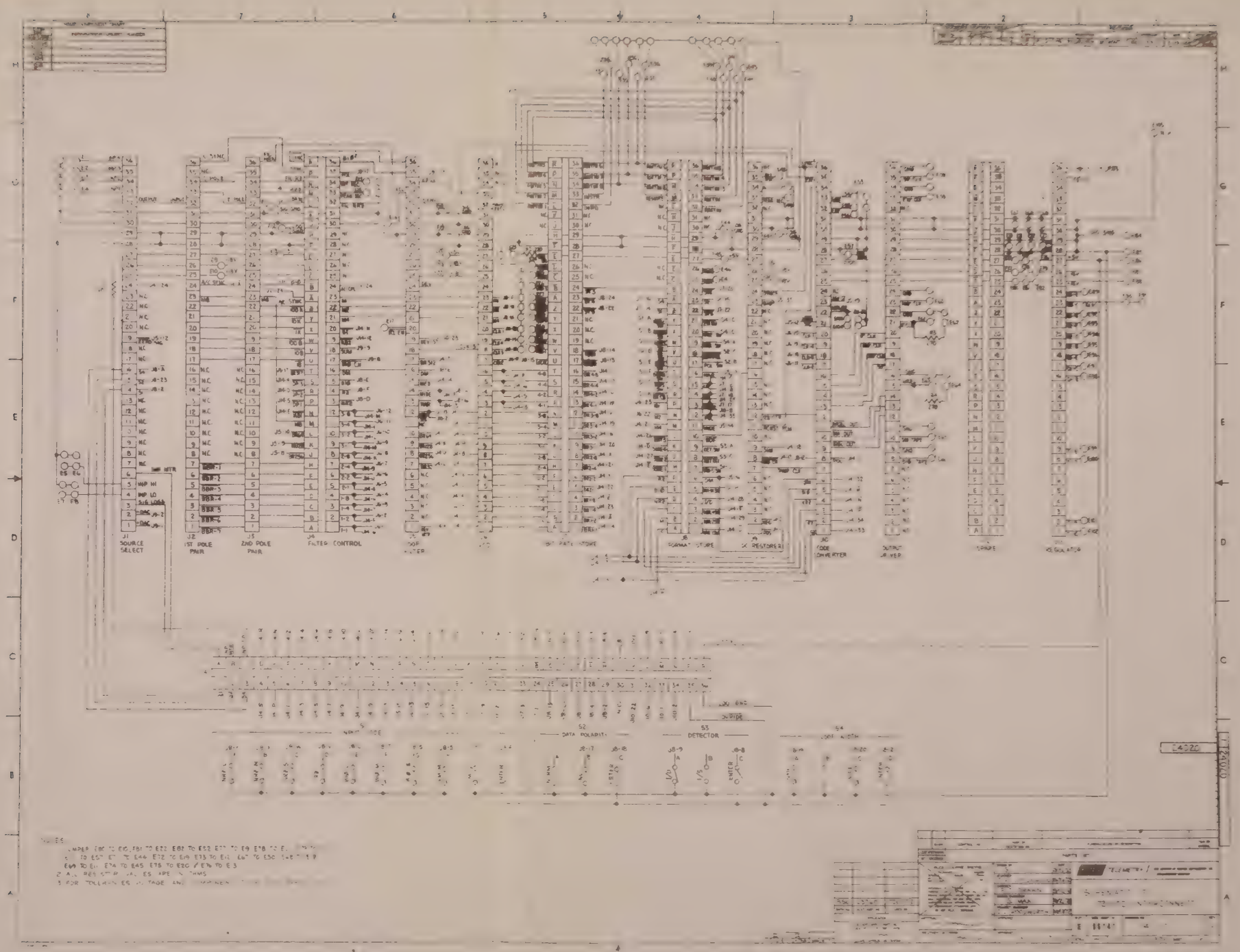
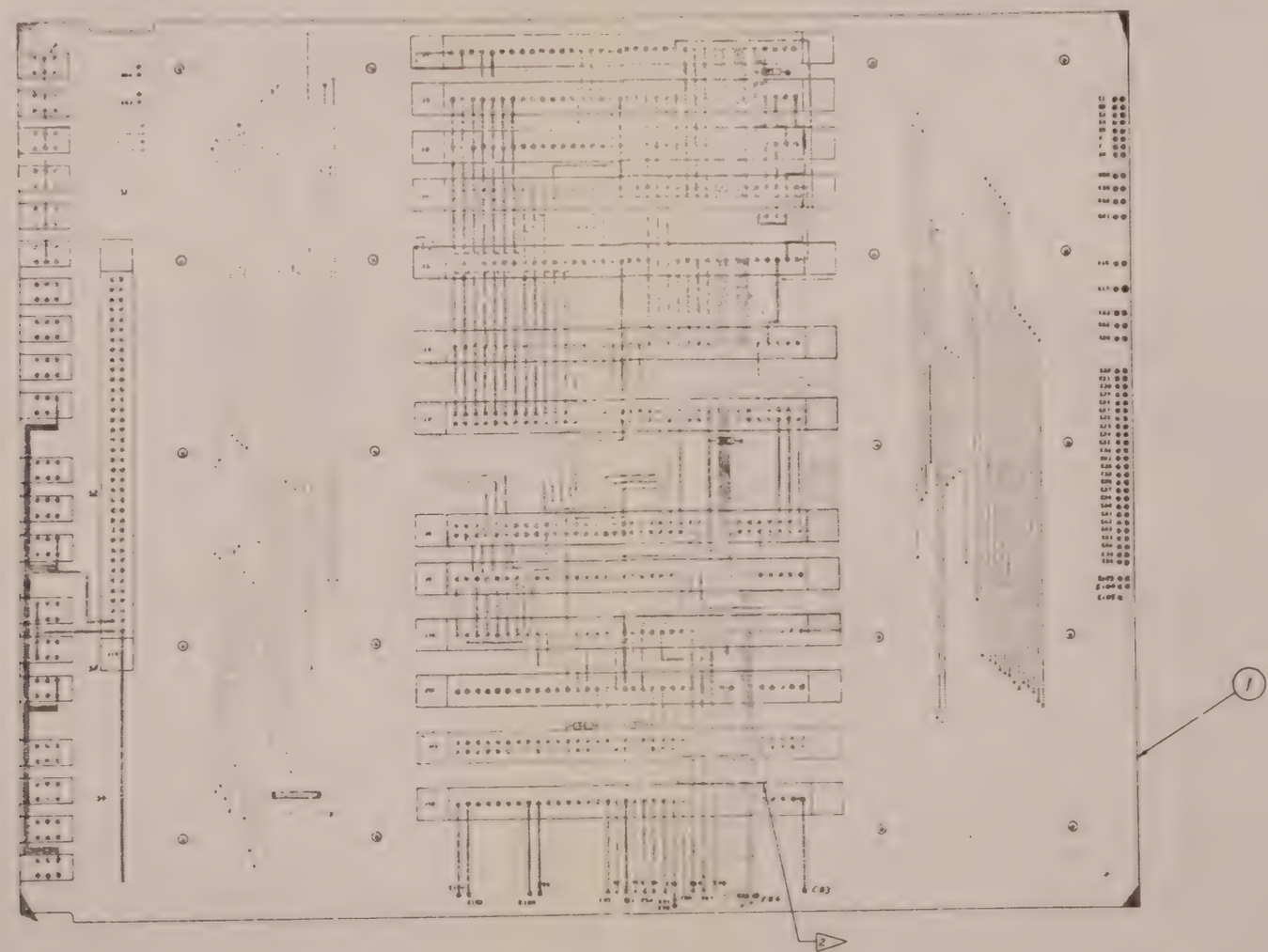


FIG 5-4
INTERCONNECTION BOARD AI
SCHEMATIC DIAGRAM



24023

NOTES

UNLESS OTHERWISE SPECIFIED.

1. MAX. HEIGHT, COMPONENT SIDE .570 ,
NON-COMPONENT SIDE [illegible] LEAD CLIPPING .093 MAX.
[illegible]

[illegible] ITEM 3 TO CONNECT E80 TO E10, E81 TO E23, E82 TO E52, E77 TO E9, E78 TO E21, E79 TO E51, E70 TO E57, E71 TO E44, E72 TO E13, E73 TO E12, E67 TO E50, E68 TO E18, E69 TO E11, E74 TO E45, E75 TO E20 & E76 TO E13 OPPOSITE SIDE OF BOARD.

[illegible] UNSUPPORTED [illegible] TO [illegible] BONDED TO PWA, [illegible] ITEM 2 AS REQUIRED.

4 USING ITEM 4 (TAPE) INSULATE REAR BRACKETS OF SWITCH 1 THRU 4 FROM CIRCUITRY AS REQD

205-89-01378		FOR PARTS LIST SEE PL- 24023
CONTROL NO		NOMENCLATURE OR DESCRIPTION

PARTS LIST

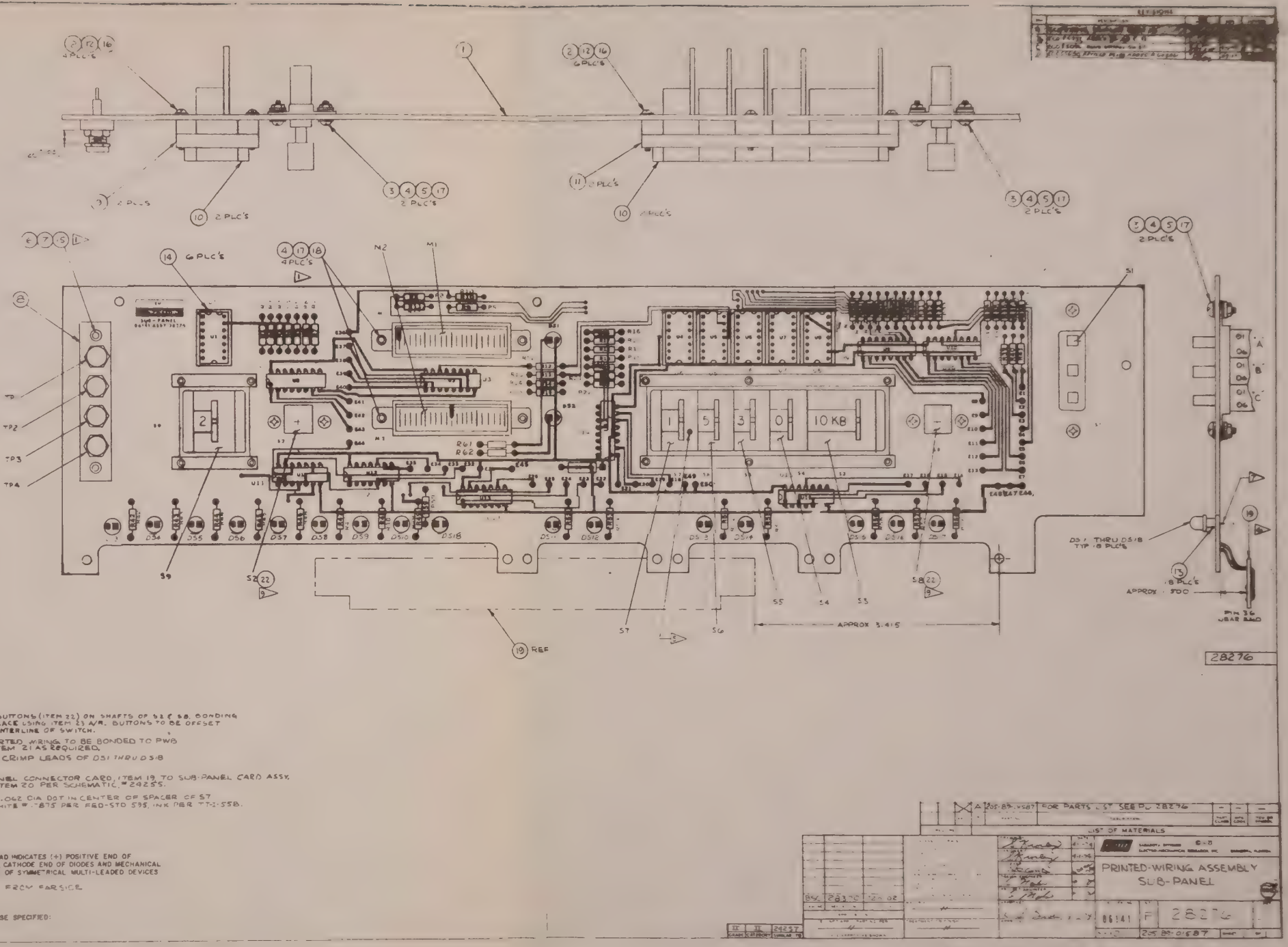
BSC	23760	720-02
DASH NO	NEXT ASSY NO	USED ON

TELEMETRY

PRINTED WIRING ASSEMBLY
INTERCONNECT
720-02

D 06141 24023

SCALE 1/1 205-89-01378



9 INSTALL BUTTONS (ITEM 22) ON SHAFTS OF S2 & S8, BONDING THEM IN PLACE USING ITEM 23 A/R. BUTTONS TO BE OFFSET ABOVE CENTERLINE OF SWITCH.

8. UNSUPPORTED WIRING TO BE BONDED TO PWB USING ITEM 21 AS REQUIRED.

7 DO NOT CRIMP LEADS OF DS1 THRU DS18

6 WIRE PANEL CONNECTOR CARD, ITEM 19 TO SUB-PANEL CARD ASSY, USING ITEM 20 PER SCHEMATIC #24255.

5 APPLY A .062 DIA DOT IN CENTER OF SPACER OF S7. COLOR WHITE #17875 PER FED-STD 595, INK PER TT-I-55B.

4

3

2 ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES

1 FASTEN FROM FARSIDE

UNLESS OTHERWISE SPECIFIED:
NOTES

A 05-89-0587 FOR PARTS LIST SEE DL 28276

LIST OF MATERIALS

PRINTED-WIRING ASSEMBLY
SUB-PANEL

86141 F 28276

24257

Figure 5-5. Front Subpanel A2 Assembly Diagram.

(Manual Rev. C)

5-13/5-14

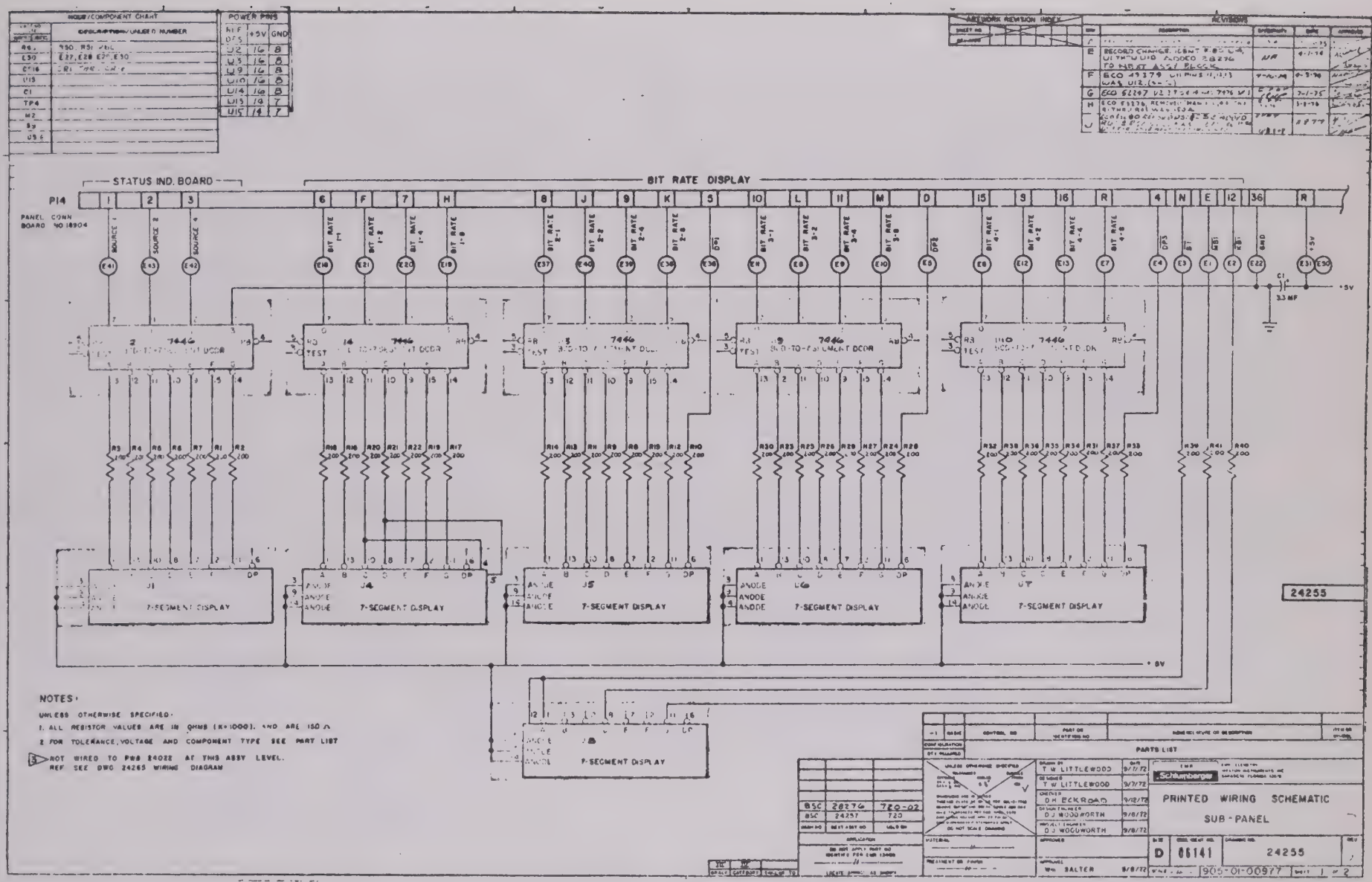


Figure 5-6 (sheet 1 of 2). Front Subpanel A2 Schematic Diagram

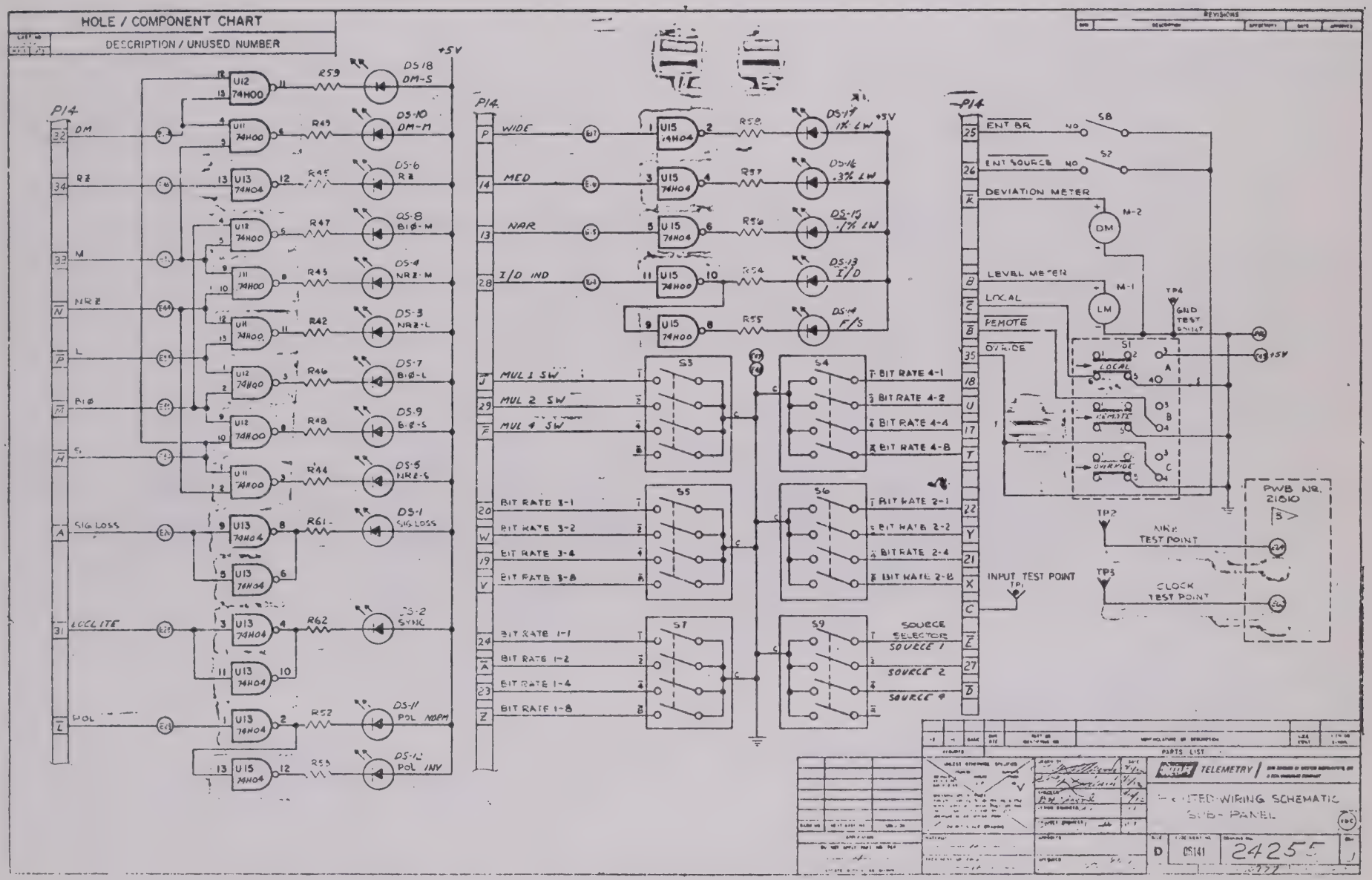


Figure 5-6 (sheet 2 of 2). Front Subpanel A2 Schematic Diagram

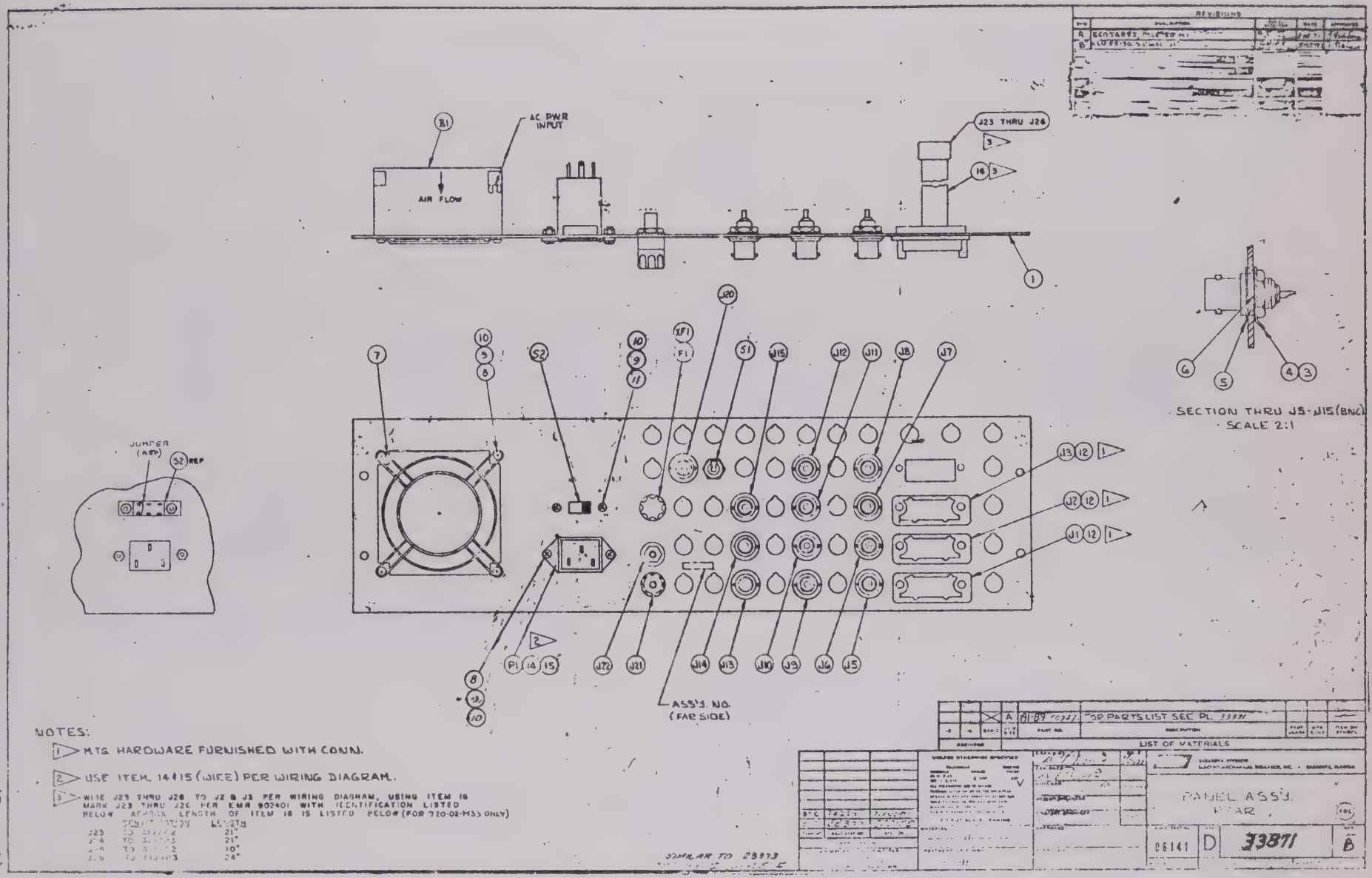


Figure 5-7. Rear Panel A4 Assembly Diagram

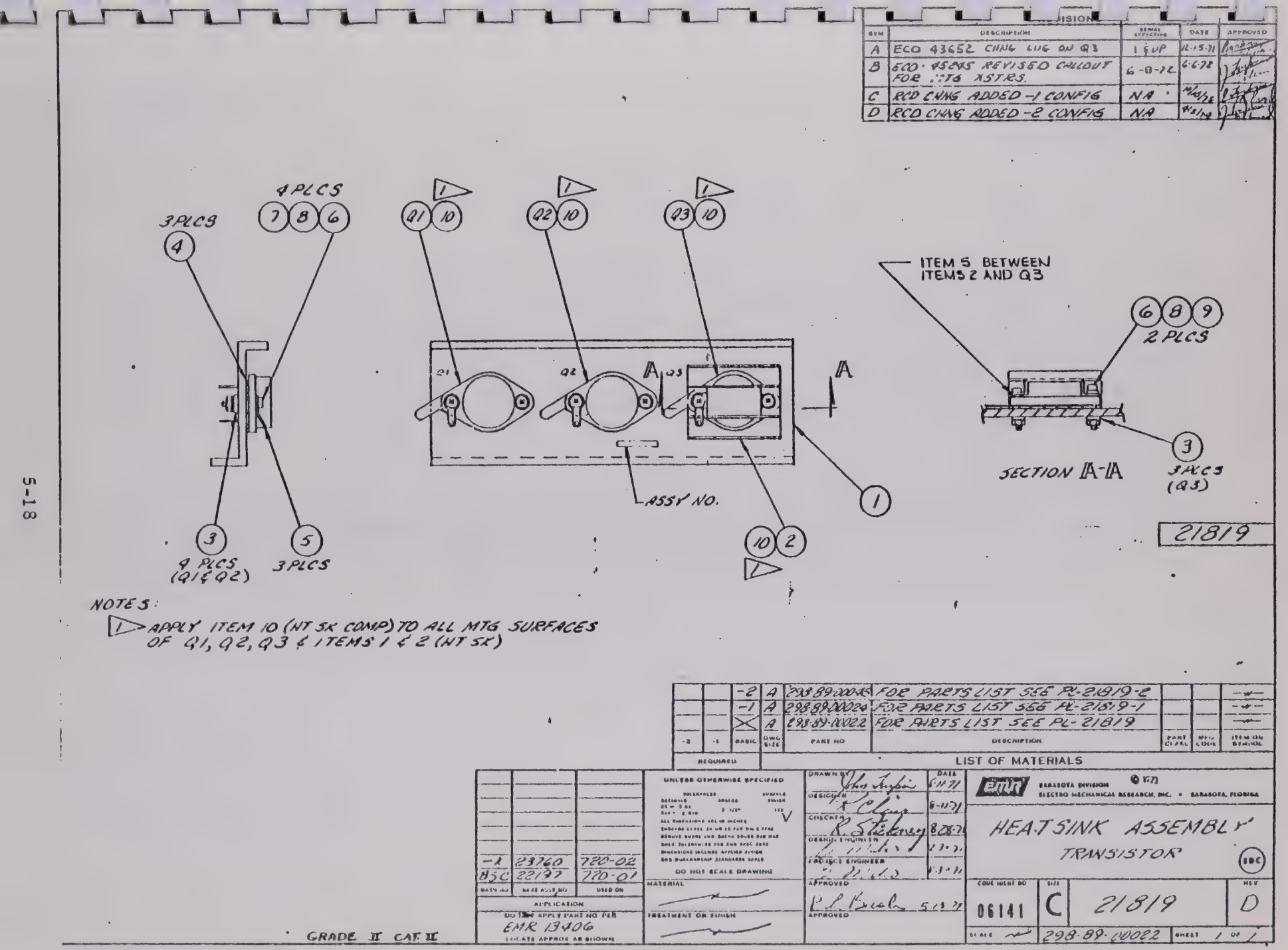


Figure 5-8. Transistor Heatsink Assembly Diagram

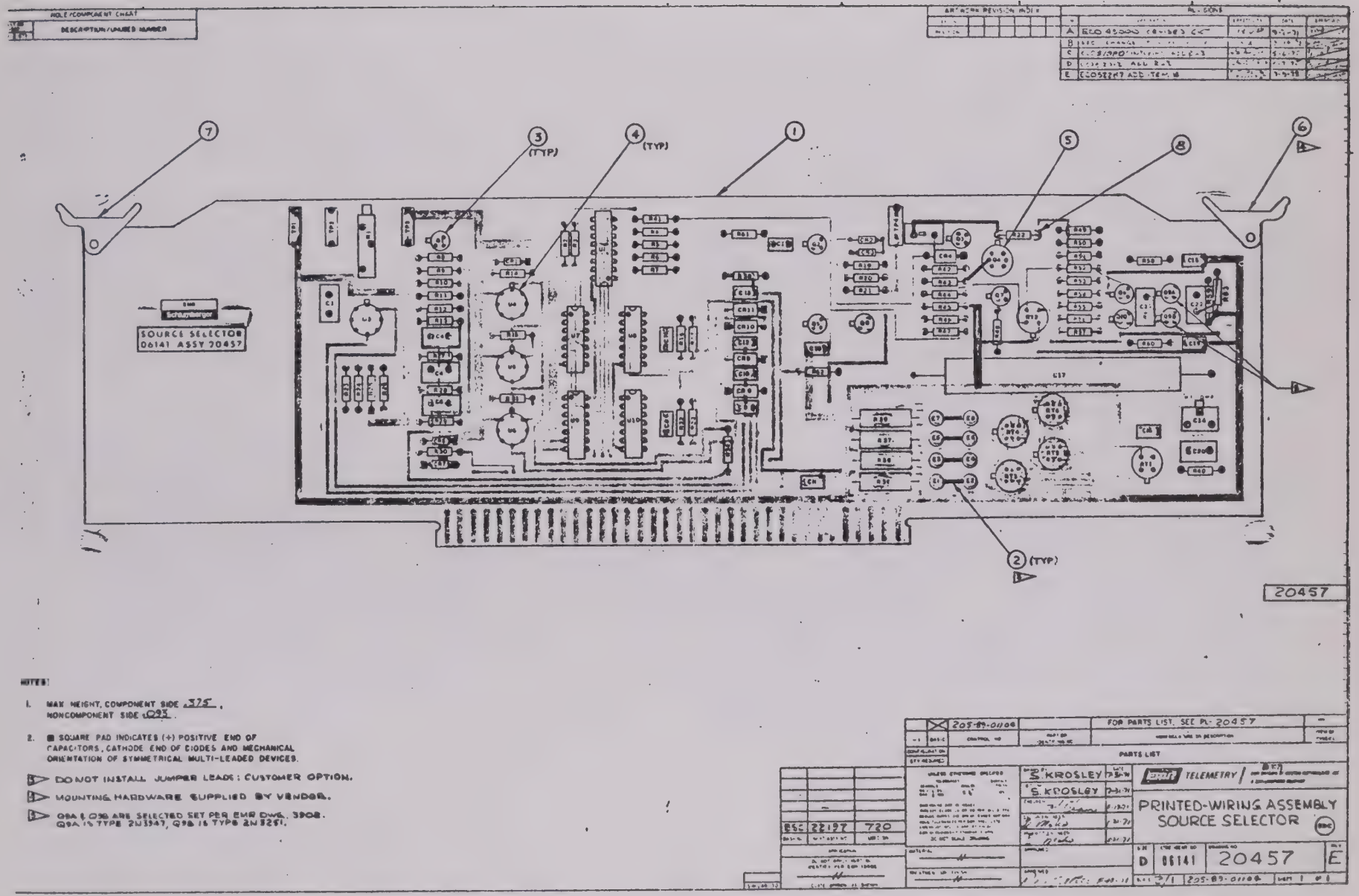


Figure 5-9. Source Select PWA (Card 1) Diagram

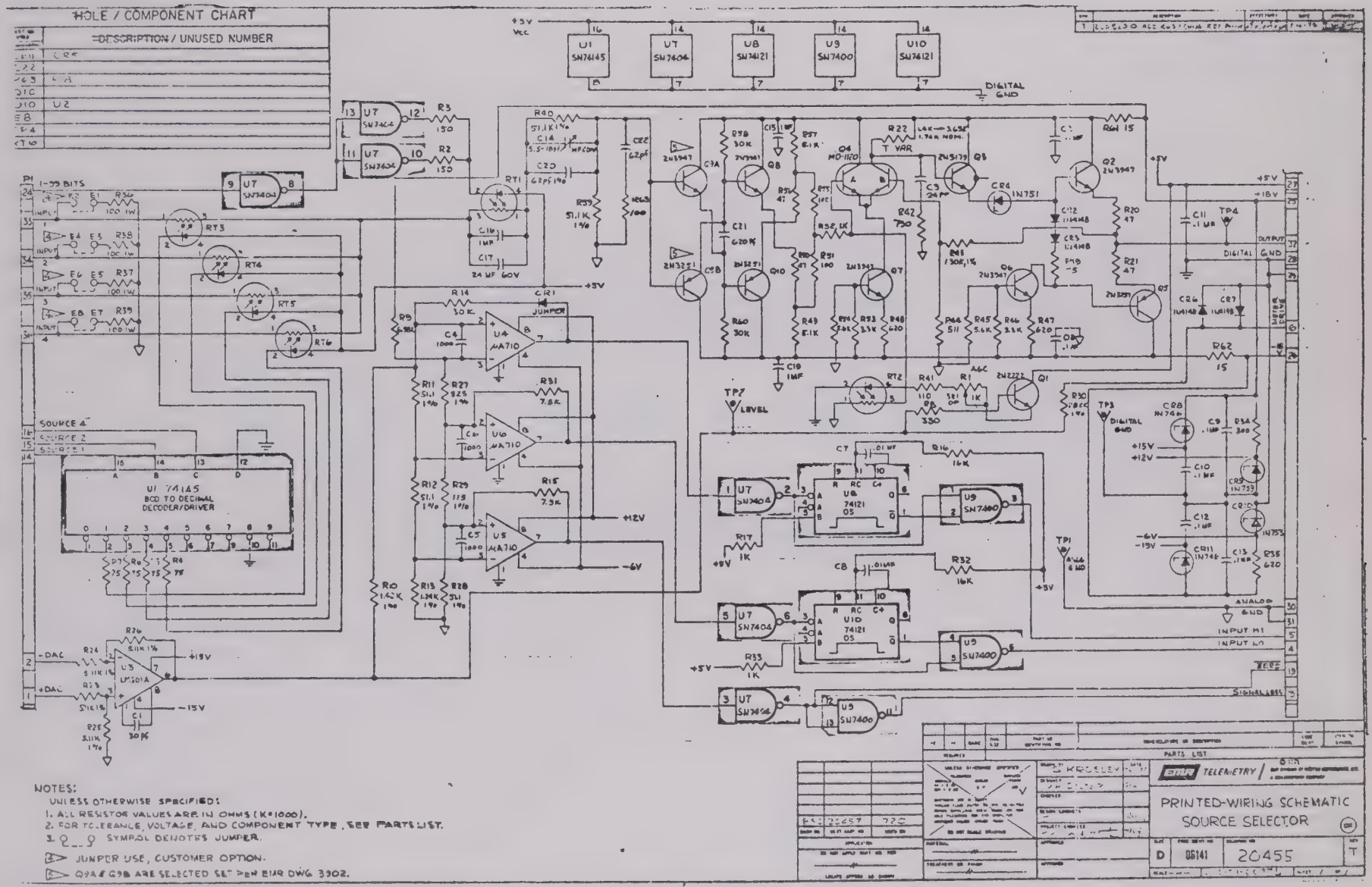


Figure 5-10 . Source Select PWA (card 1) Schematic Diagram

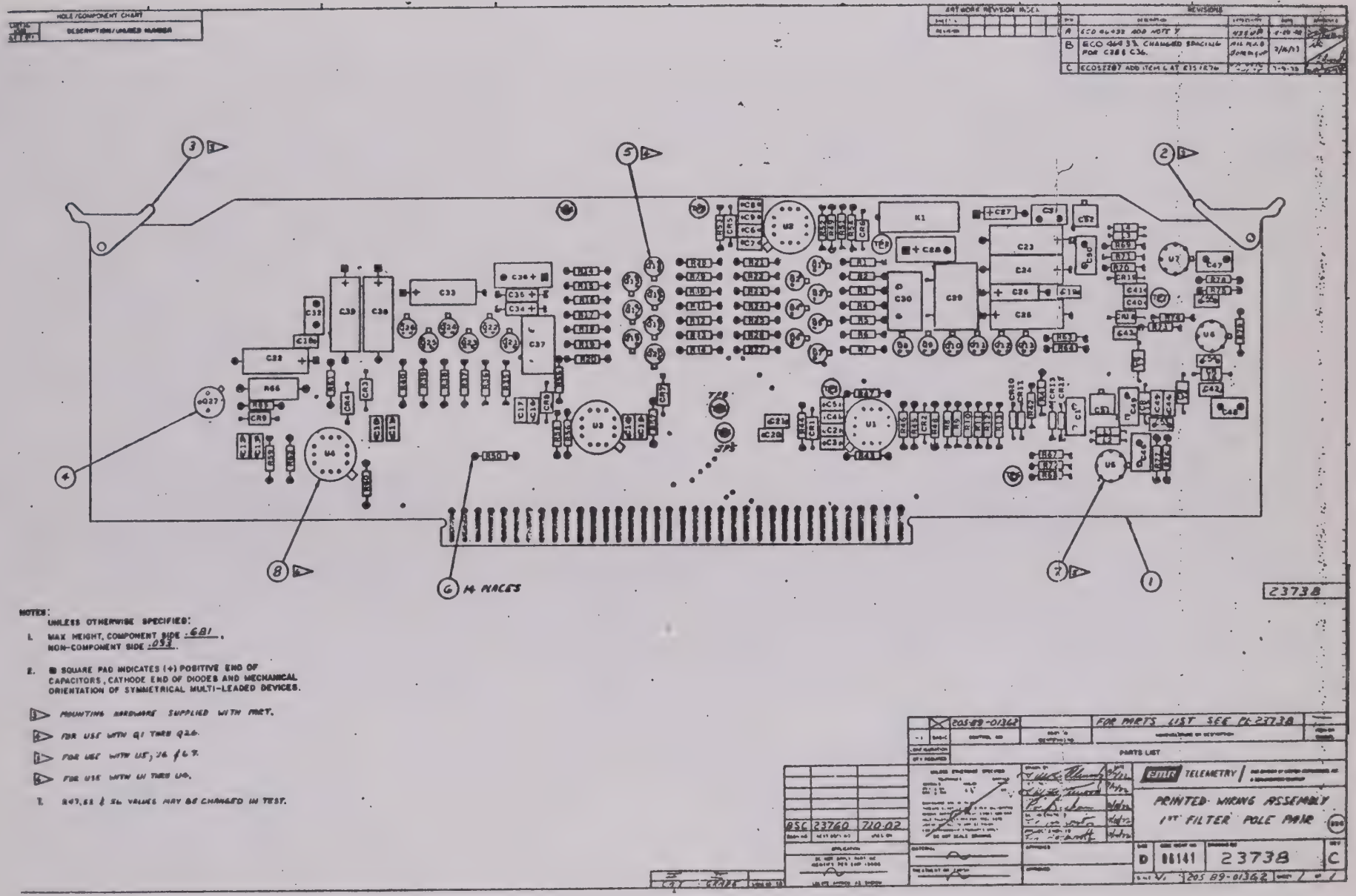


Figure 5-11. First Filter Pole Pair PWA (Card 2) Diagram

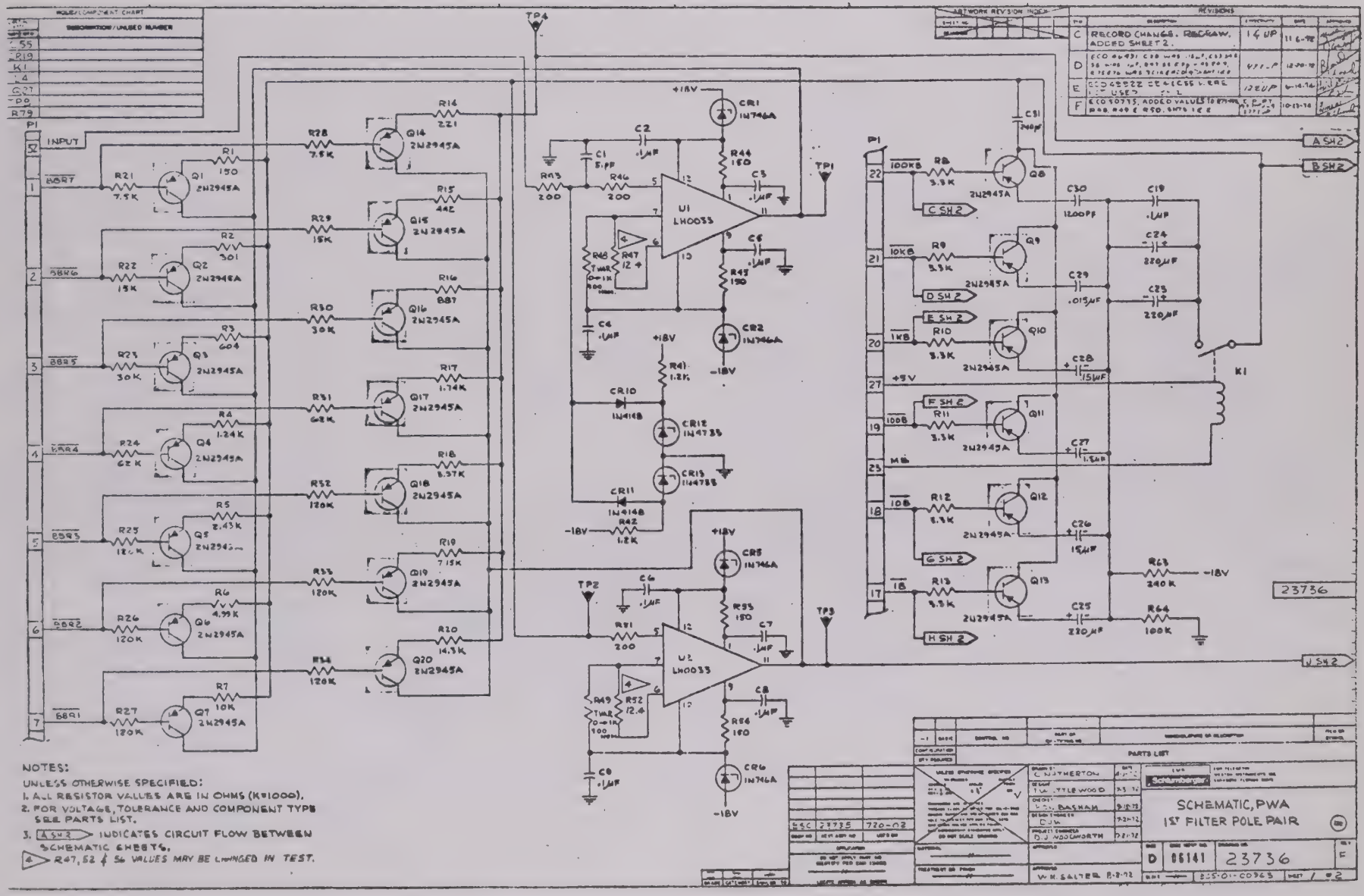


Figure 5-12 (Sheet 1 of 2). First Filter Pole Pair PWA (Card 2) Schematic Diagram

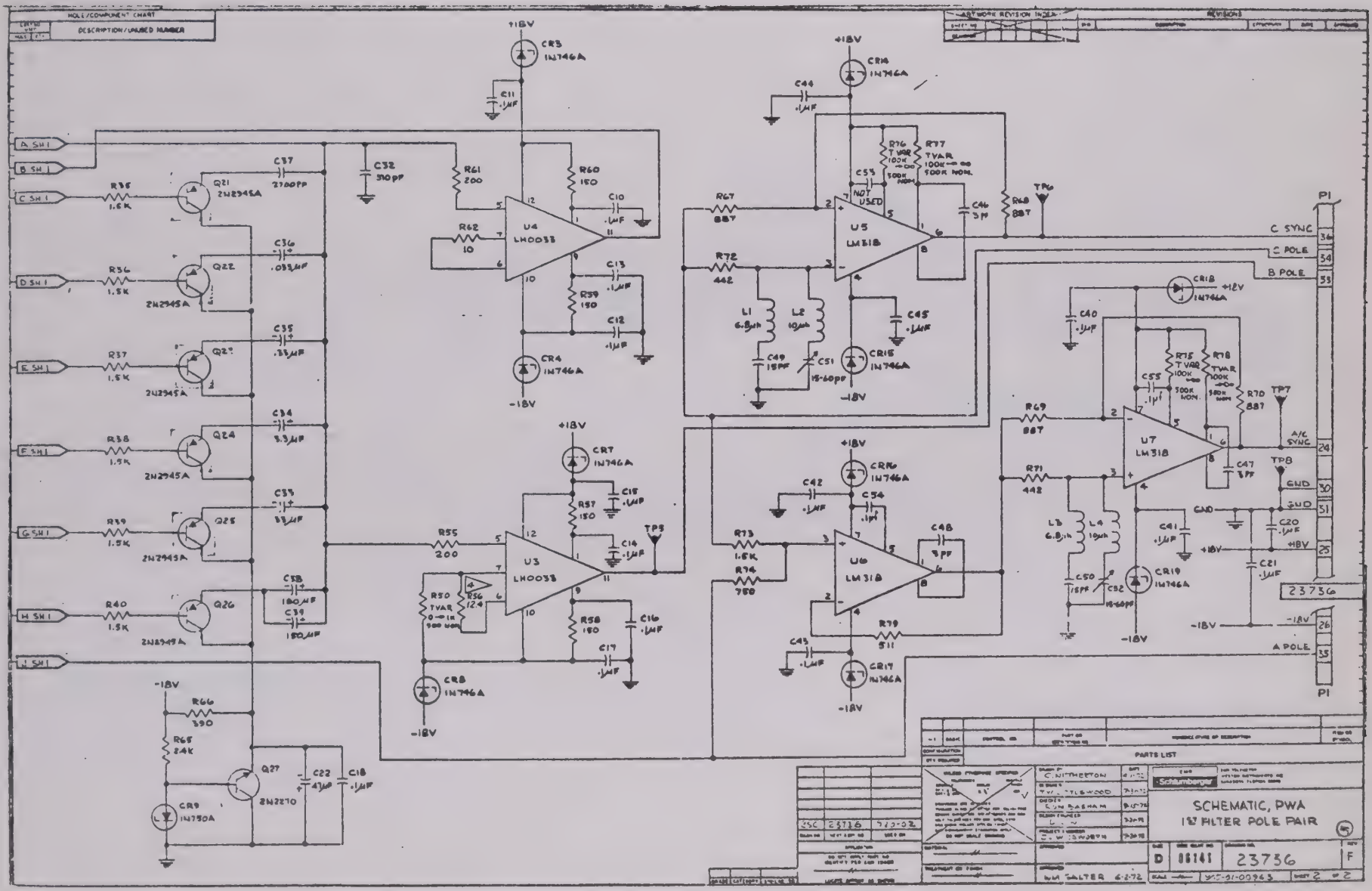


Figure 5-12 (Sheet 2 of 2). First Filter Pole PWA (Card 2) Schematic Diagram

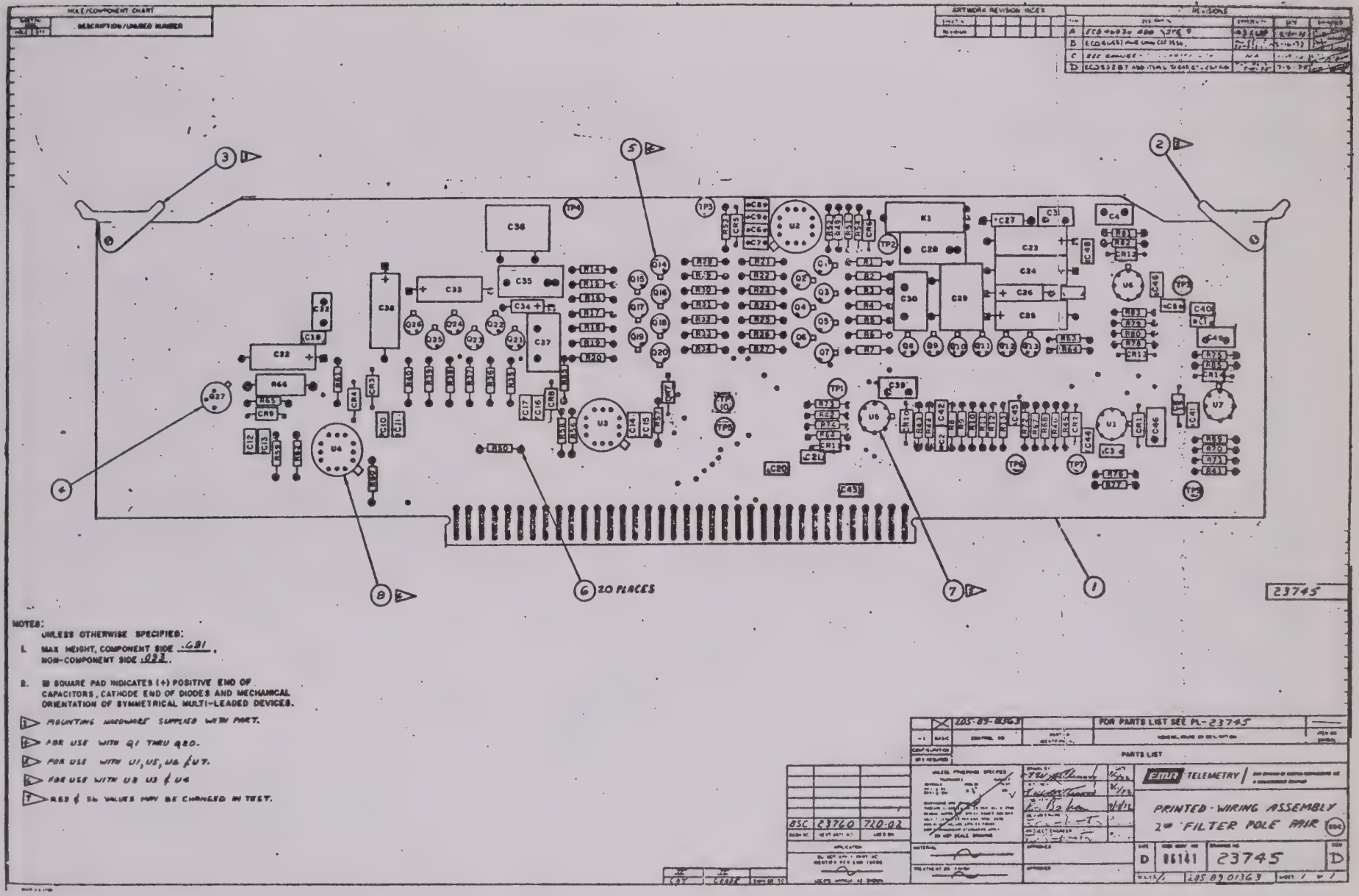


Figure 5-13. Second Filter Pole Pair PWA (Card 2) Diagram

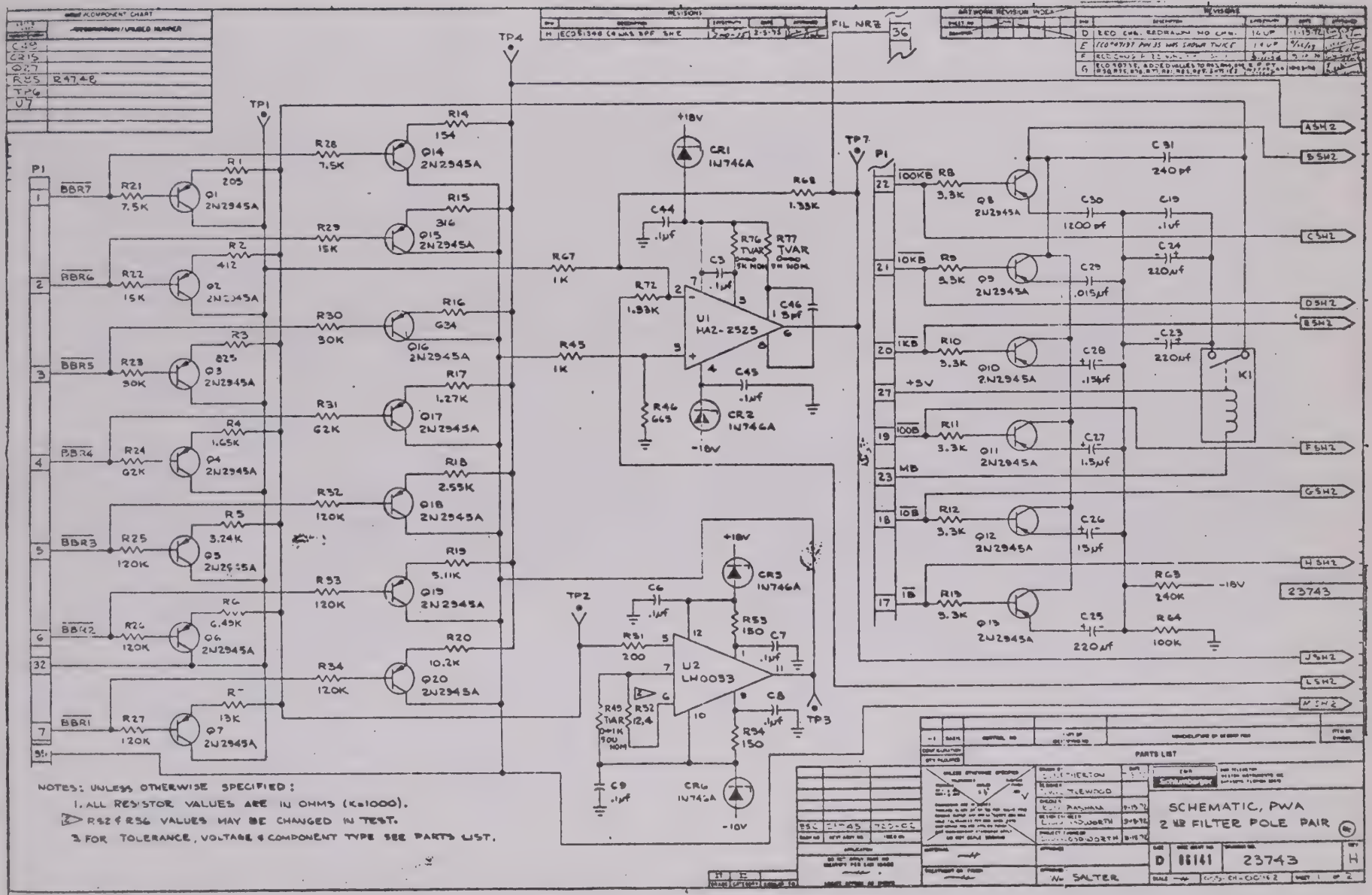


Figure 5-14 (Sheet 1 of 2). Second Filter Pole Pair PWA (Card 3) Schematic Diagram

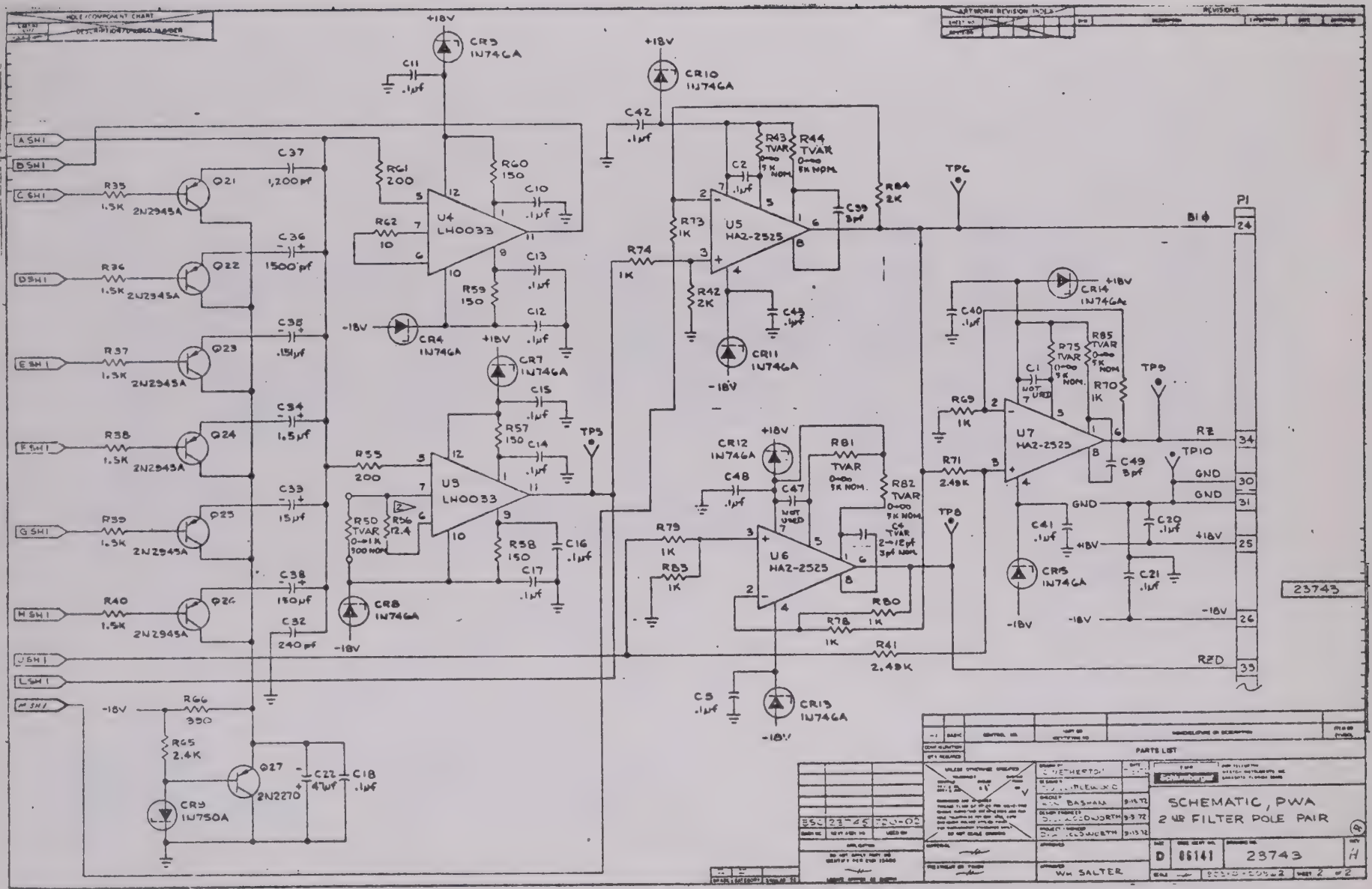


Figure 5-14 (Sheet 2 of 2). Second Filter Pole Pair PWA (Card 3) Schematic Diagram

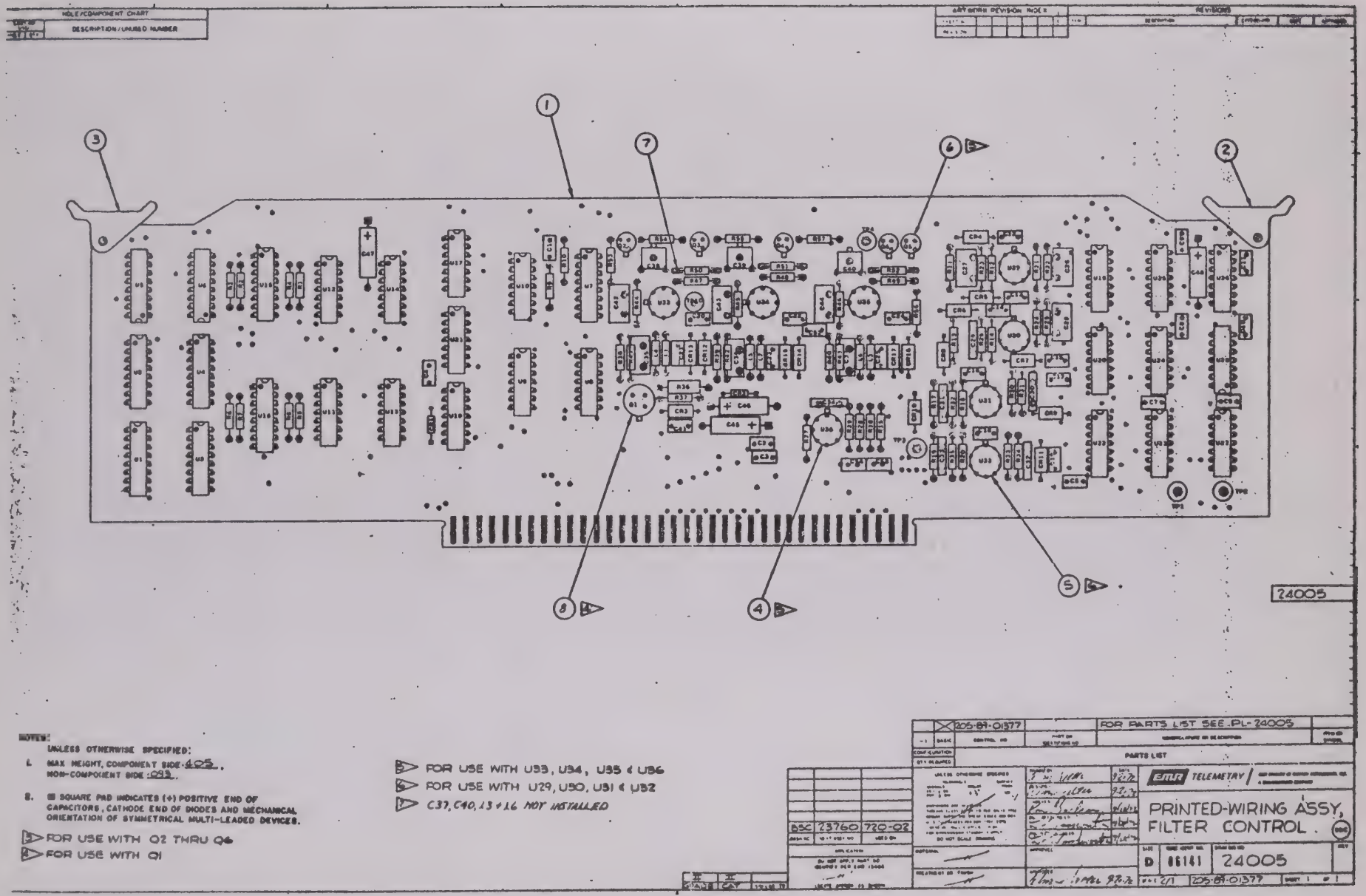


Figure 5-15. Filter Control PWA (Card 4) Diagram

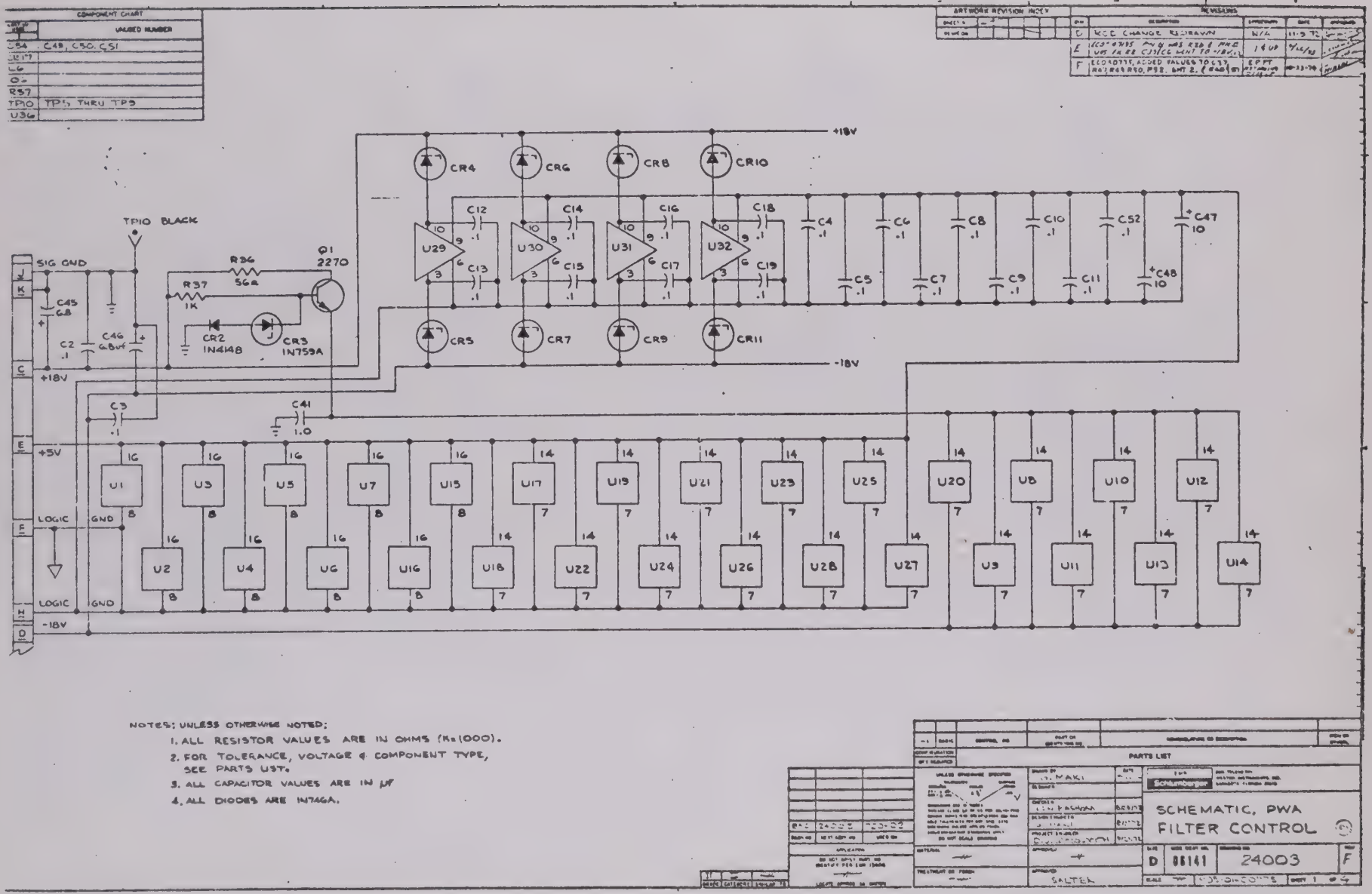


Figure 5-16 (Sheet 1 of 4). Filter Control PWA (Card 4) Schematic Diagram

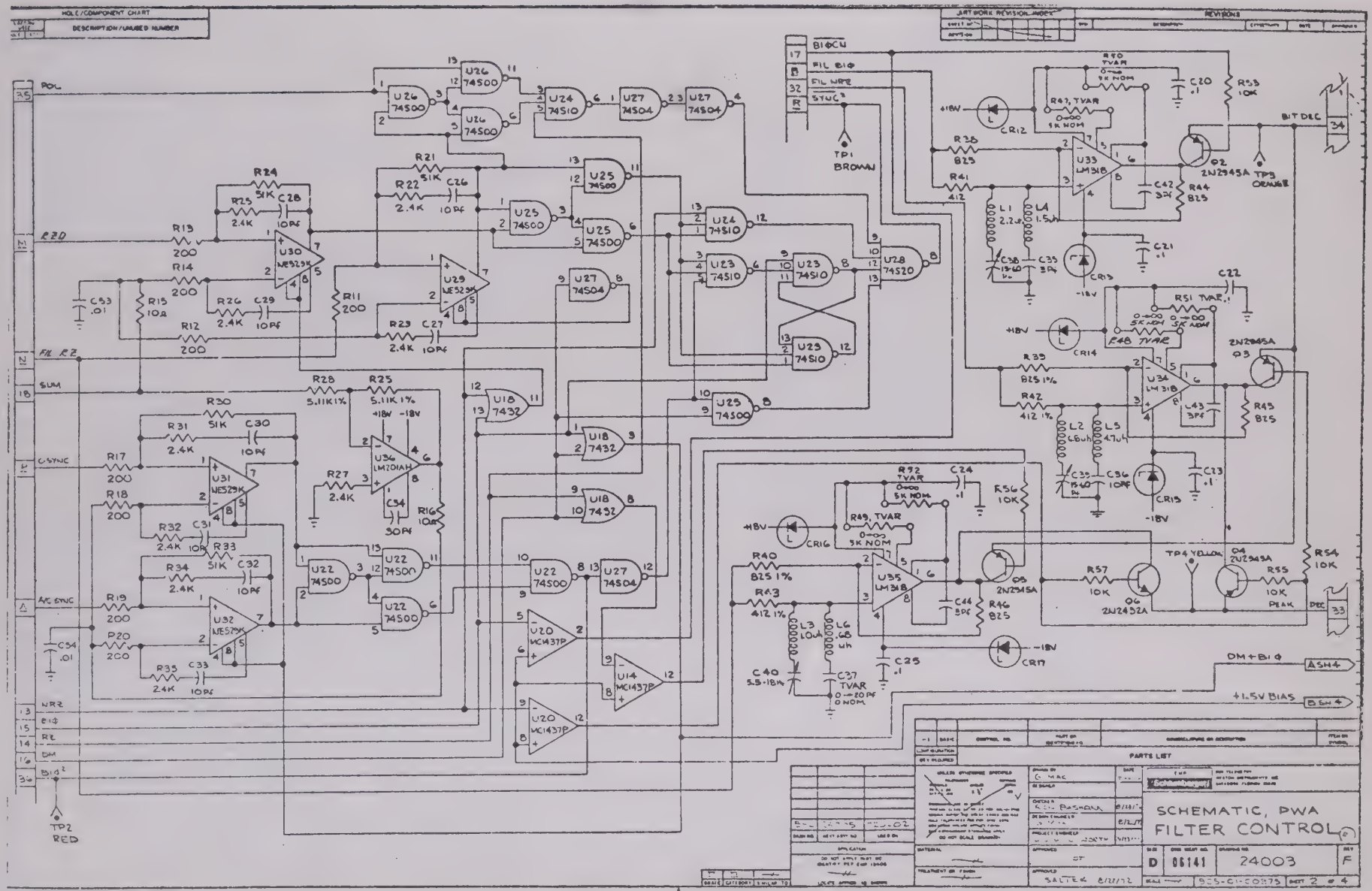


Figure 5-16 (Sheet 2 of 4). Filter Control PWA (Card 4) Schematic Diagram

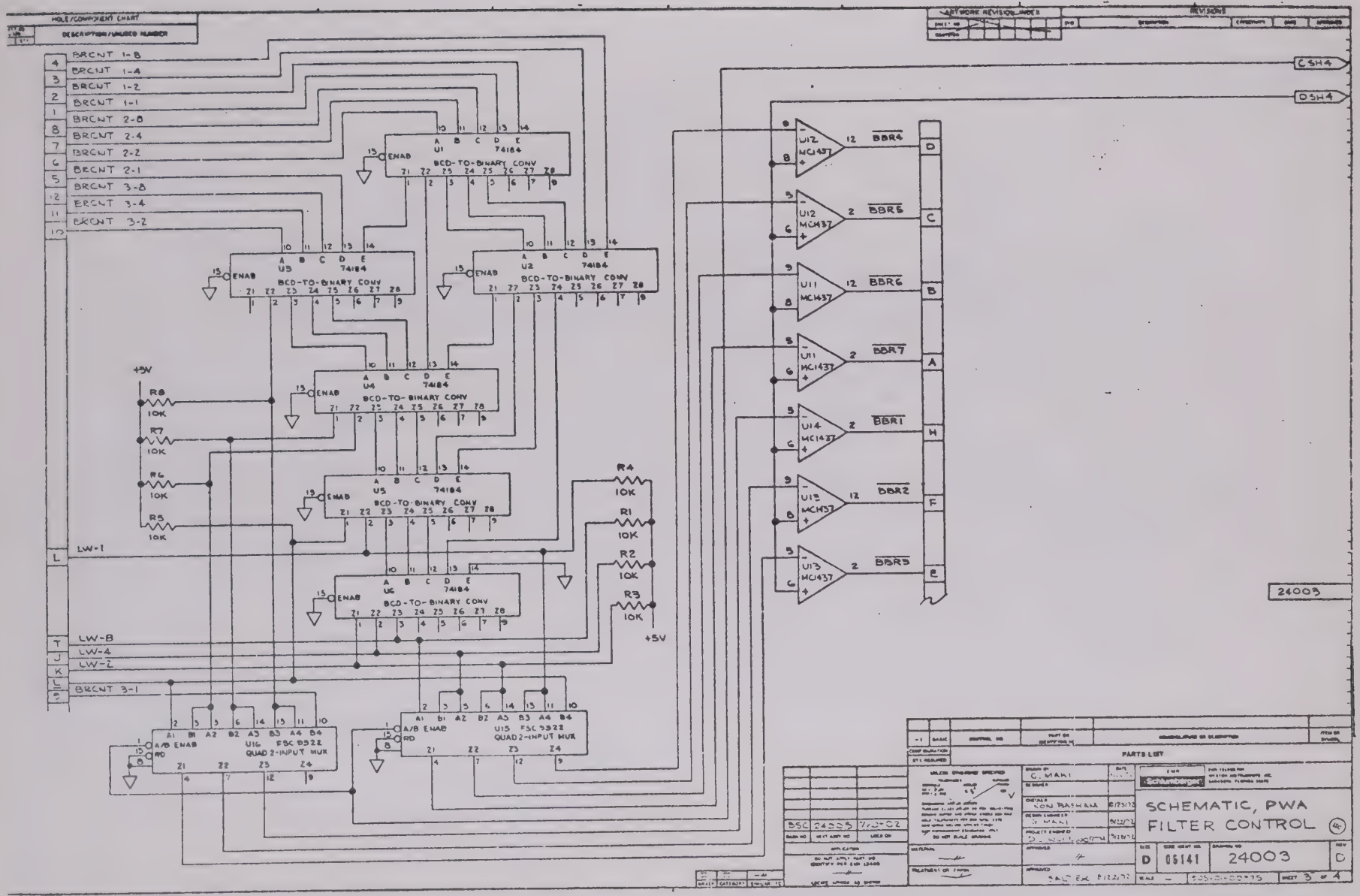


Figure 5-16 (Sheet 3 of 4). Filter Control PWA (Card 4) Schematic Diagram

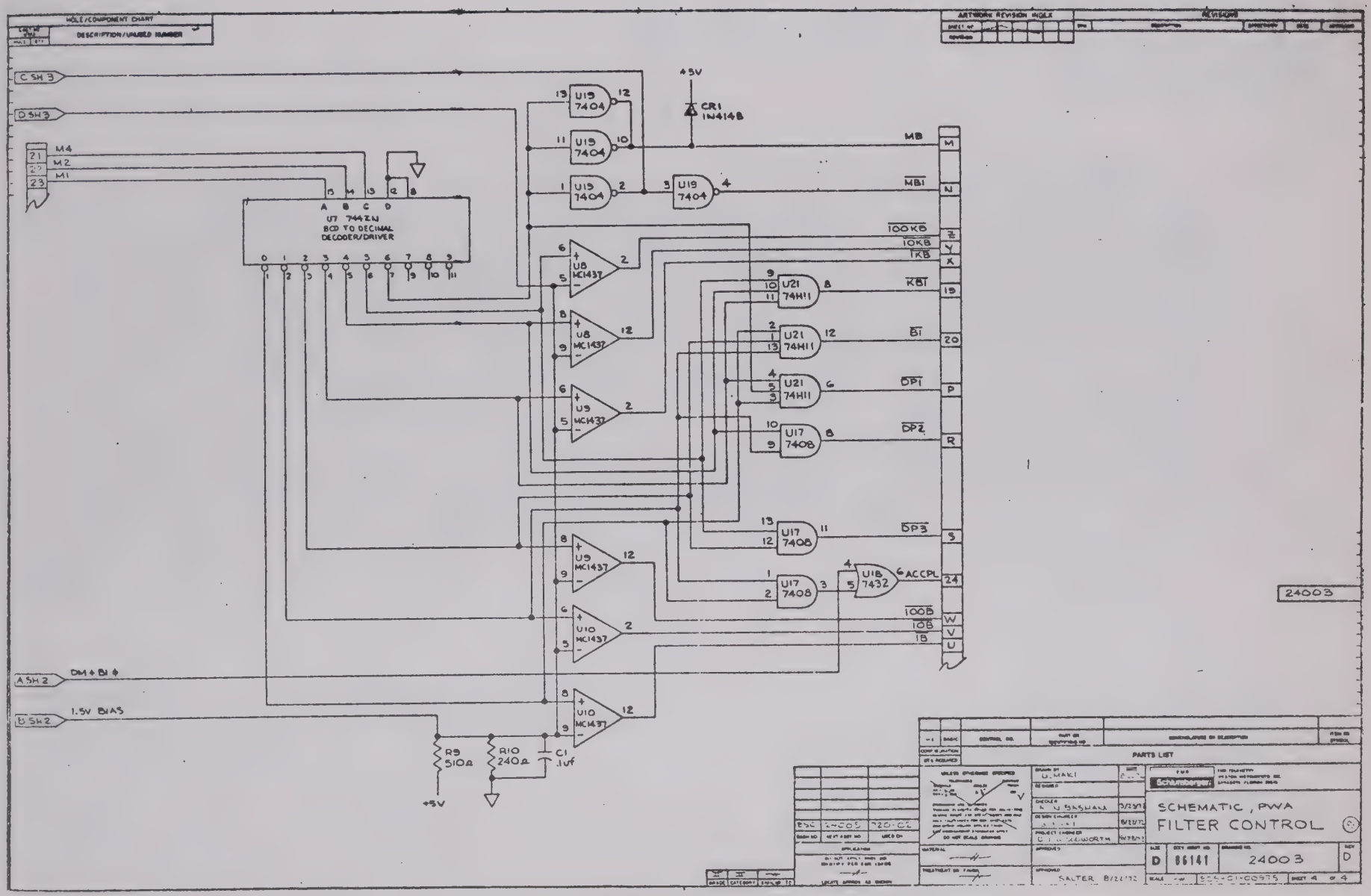


Figure 5-16 (Sheet 4 of 4). Filter Control PWA (Card 4) Schematic Diagram

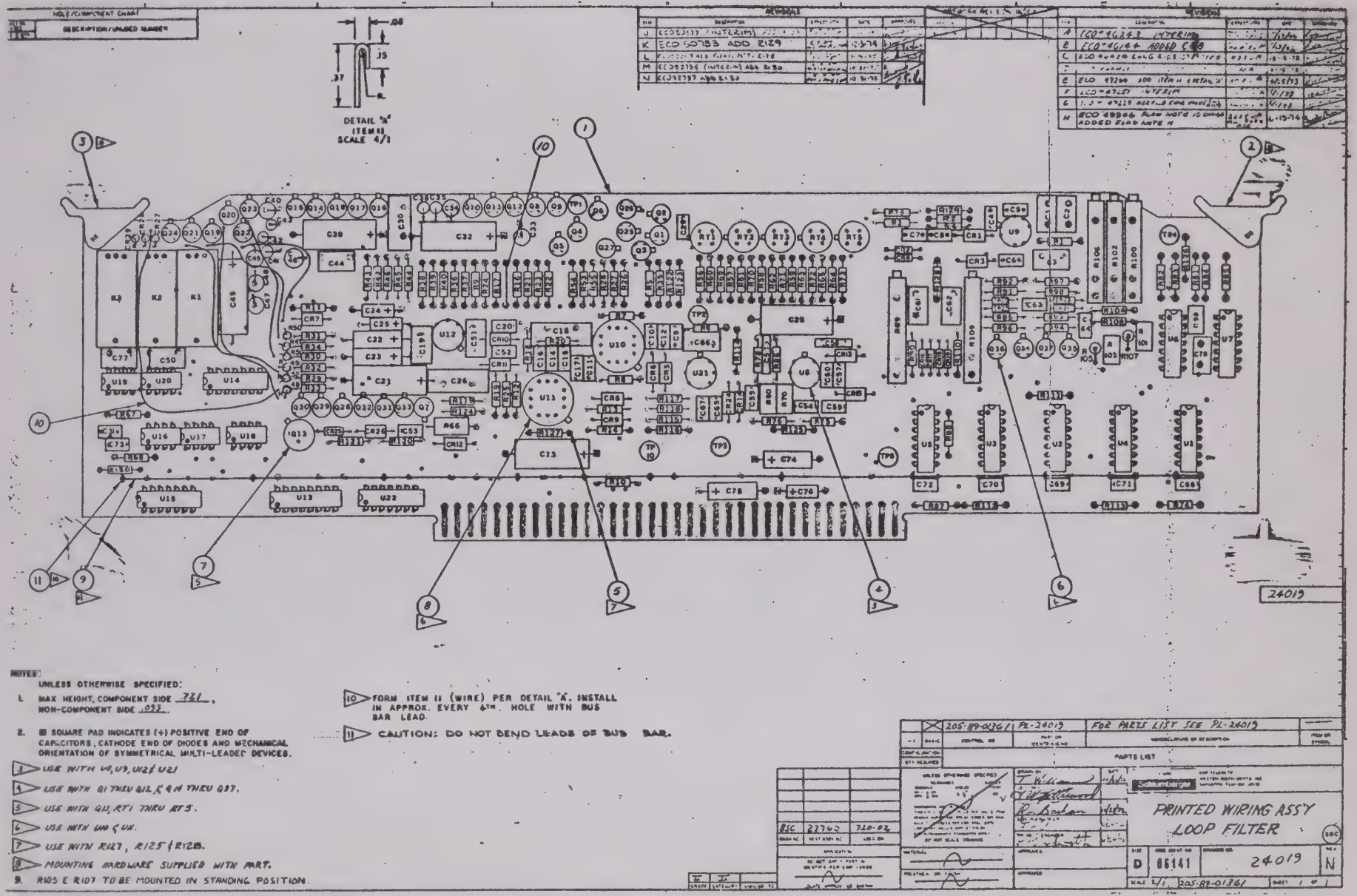


Figure 5-17. Loop Filter PWA (Card 5) Diagram

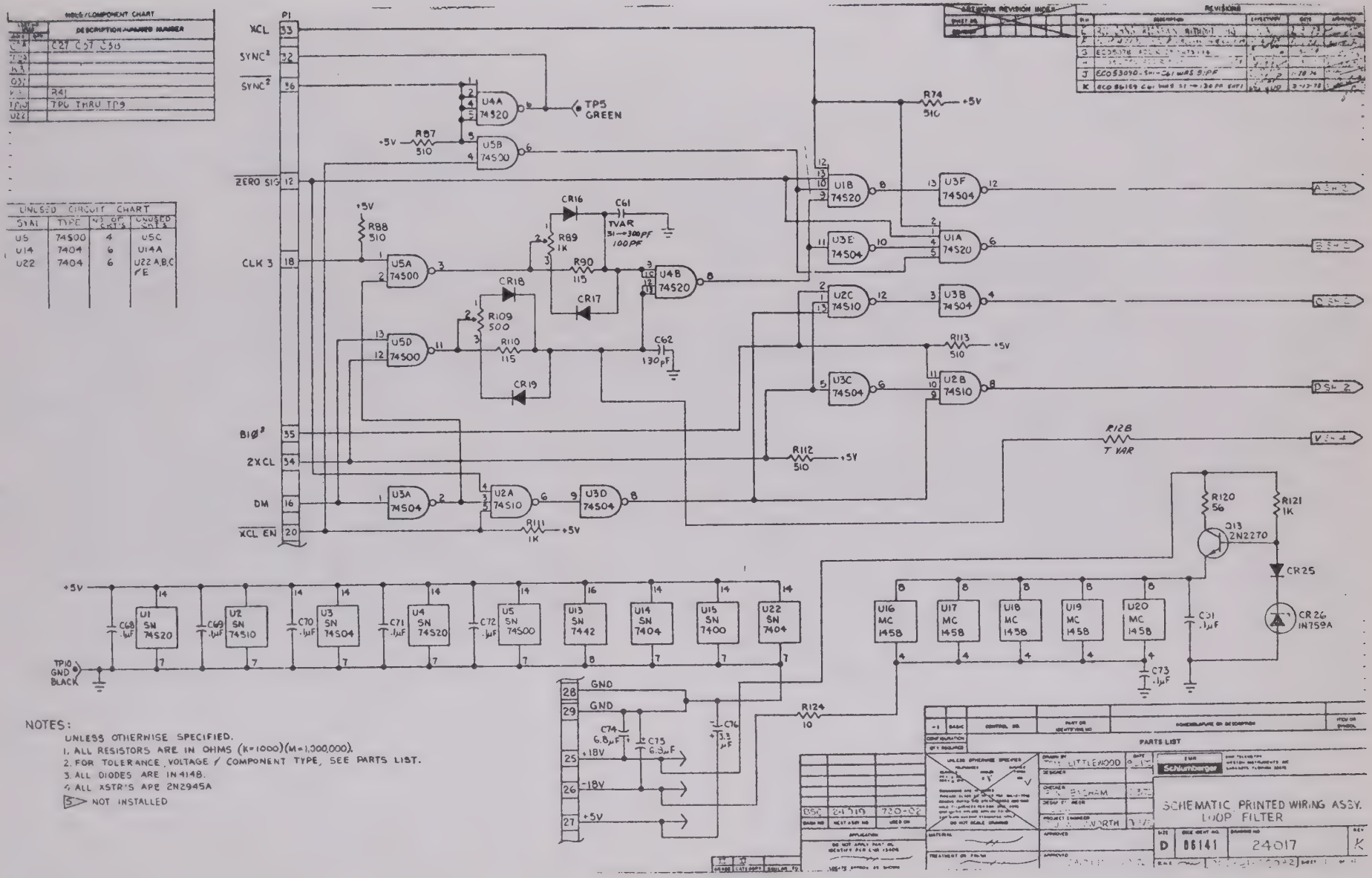


Figure 5-18 (Sheet 1 of 4). Loop Filter PWA (Card 5) Schematic Diagram

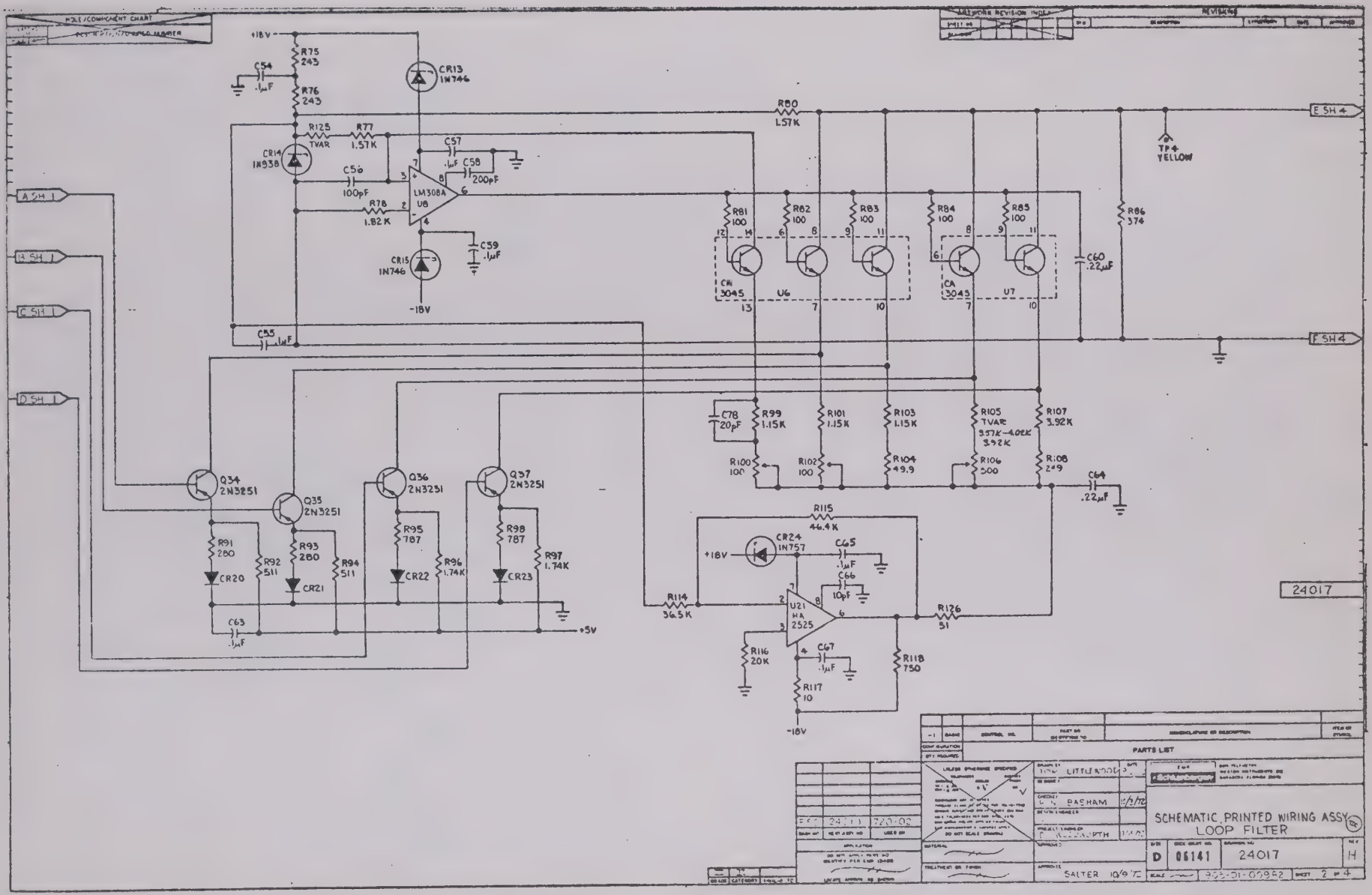


Figure 5-18 (Sheet 2 of 4). Loop Filter PWA (Card 5) Schematic Diagram

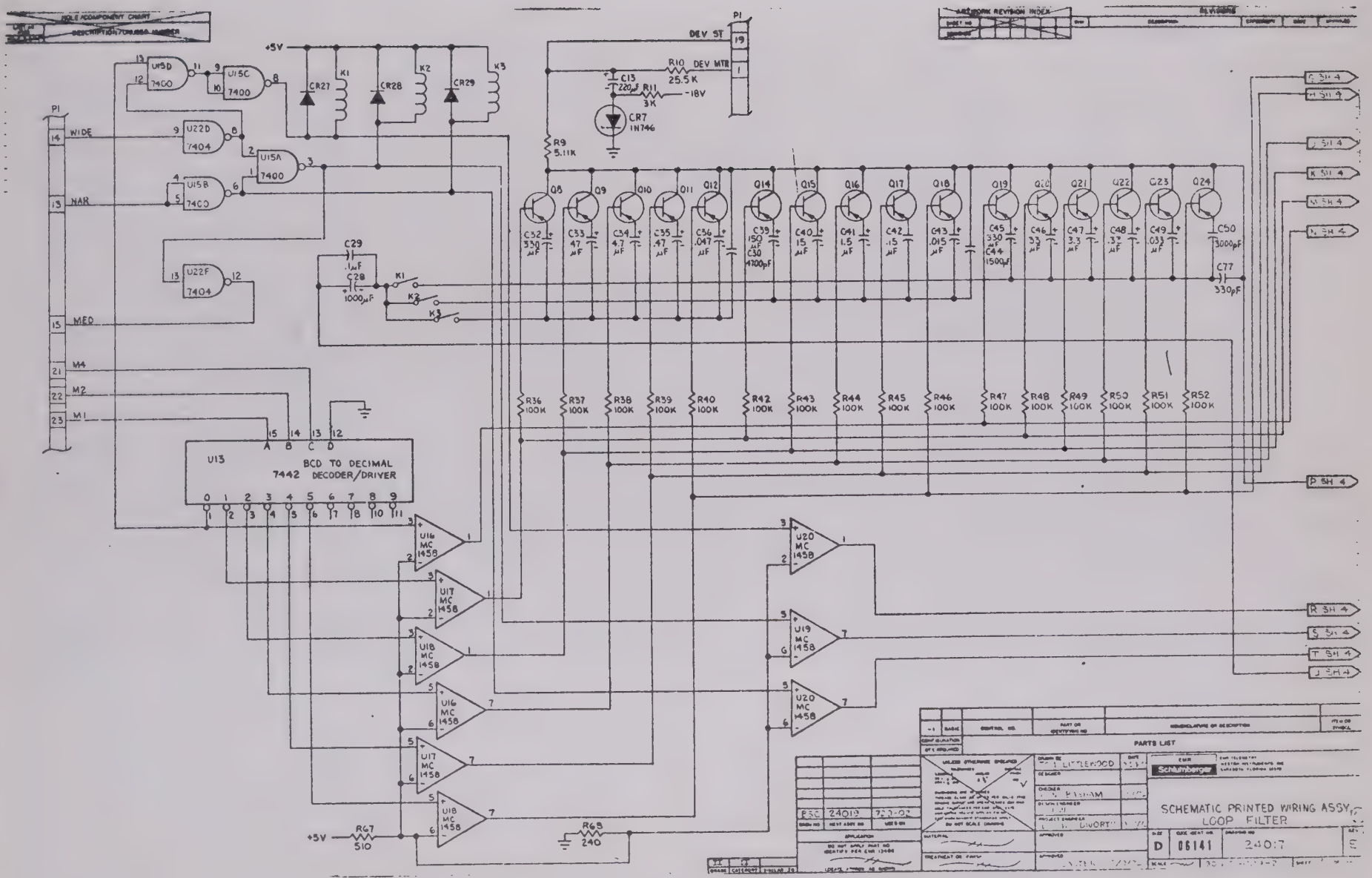


Figure 5-18 (Sheet 3 of 4). Loop Filter PWA (Card 5) Schematic Diagram

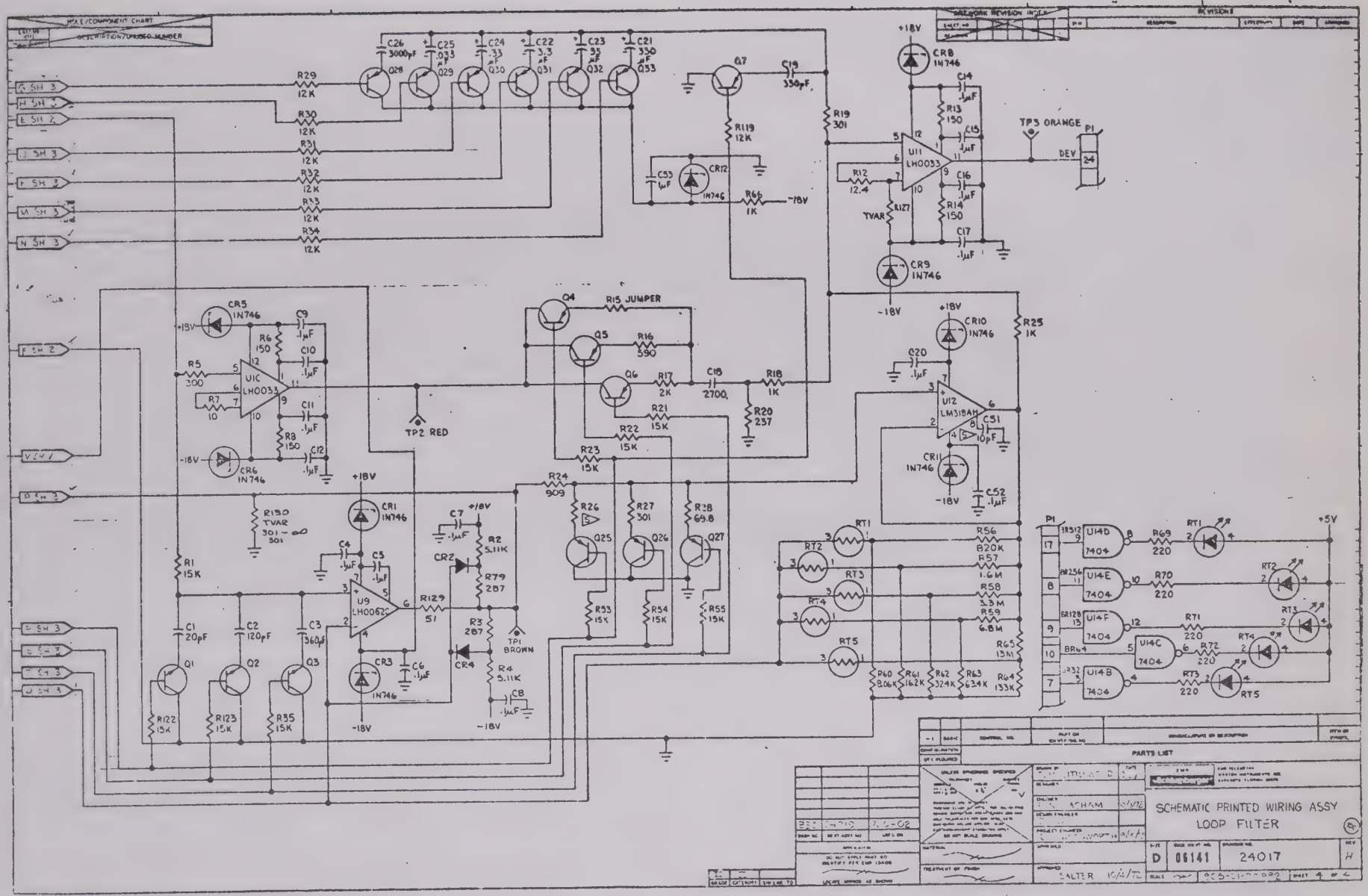


Figure 5-18 (Sheet 4 of 4). Loop Filter PWA (Card 5) Schematic Diagram

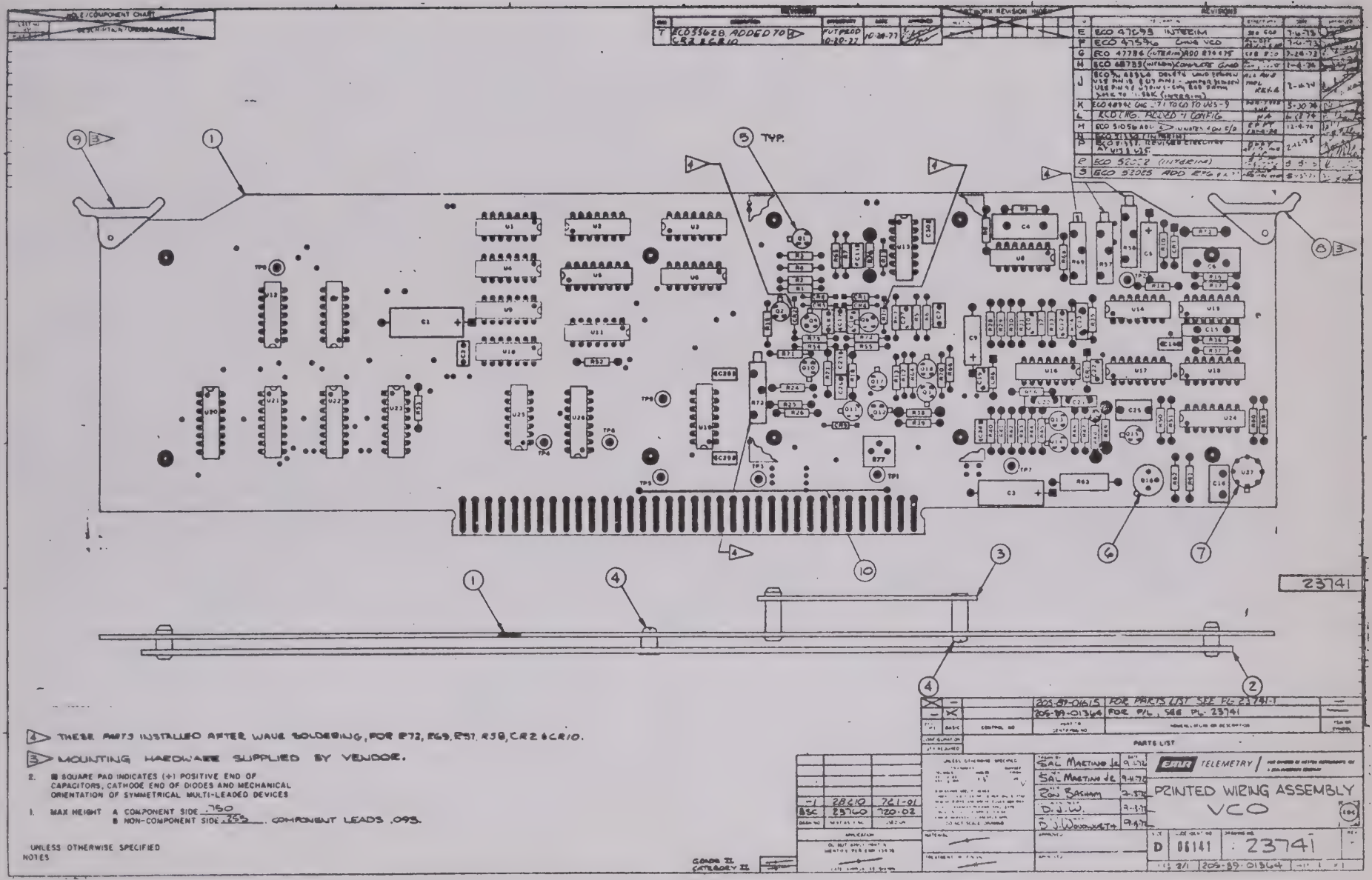


Figure 5-19. VCO PWA (Card 6) Diagram

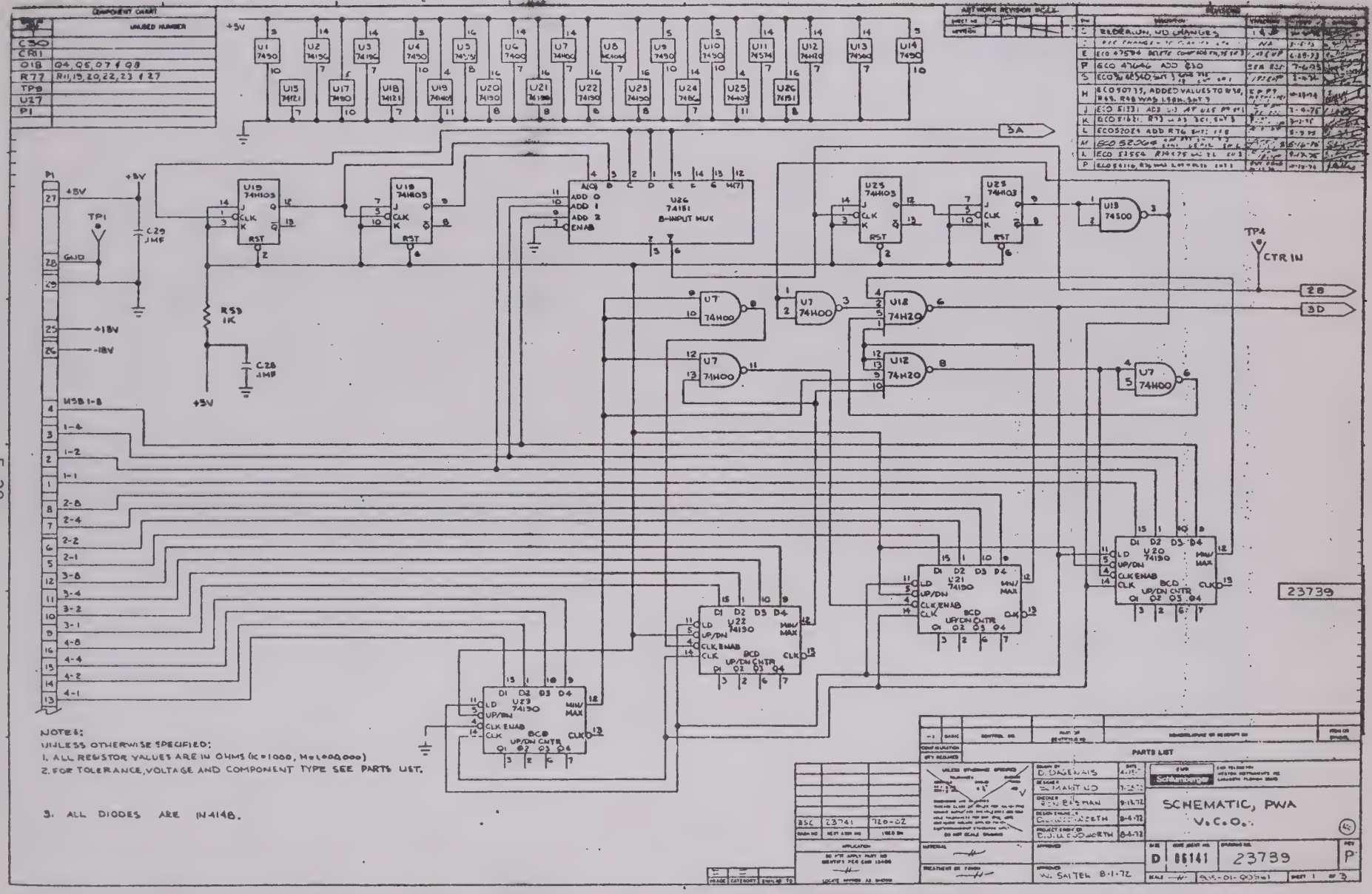


Figure 5-20 (Sheet 1 of 3). VCO PWA (Card 6) Schematic Diagram

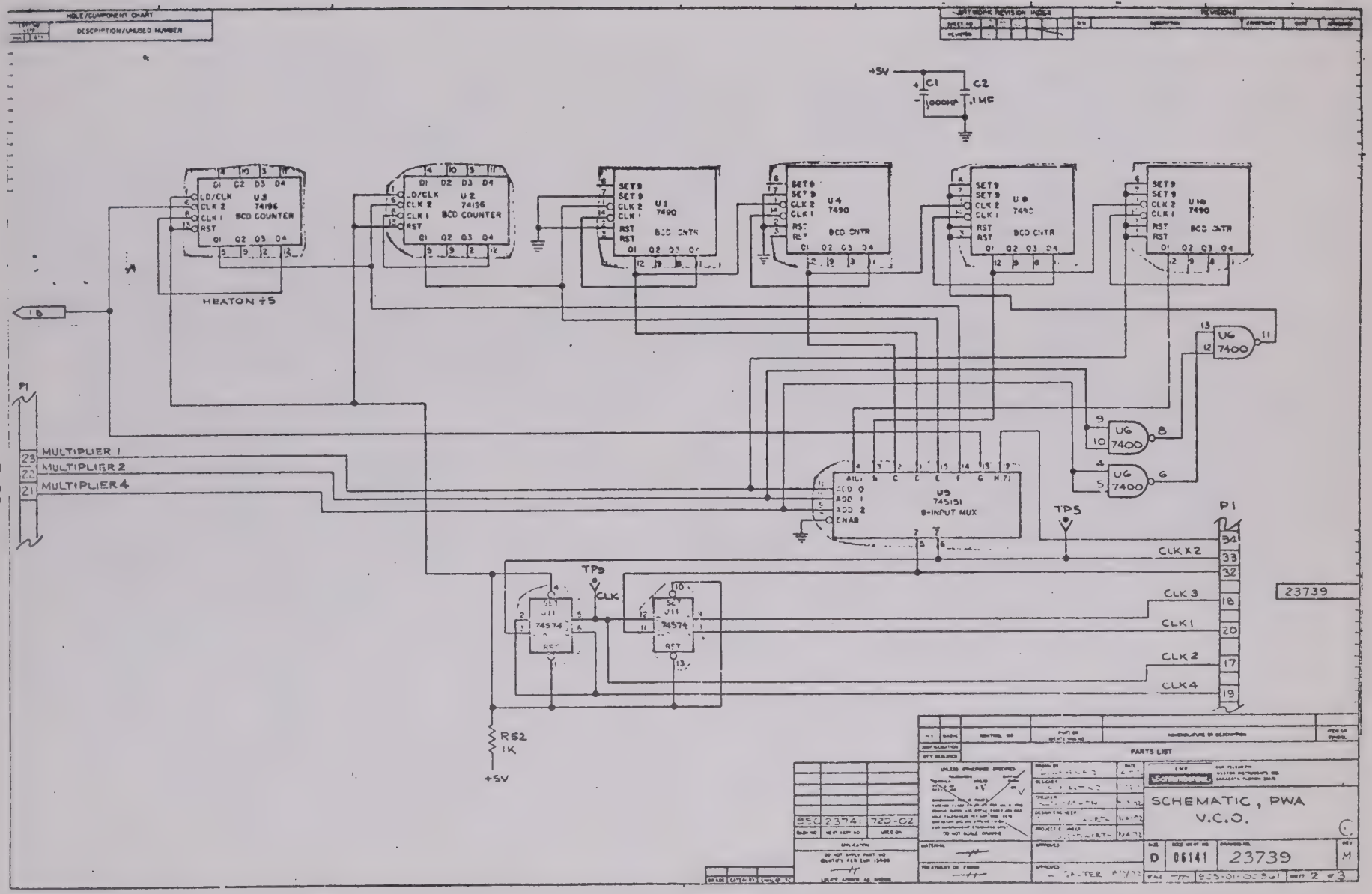


Figure 5-20 (Sheet 2 of 3). VCO PWA (Card 6) Schematic Diagram

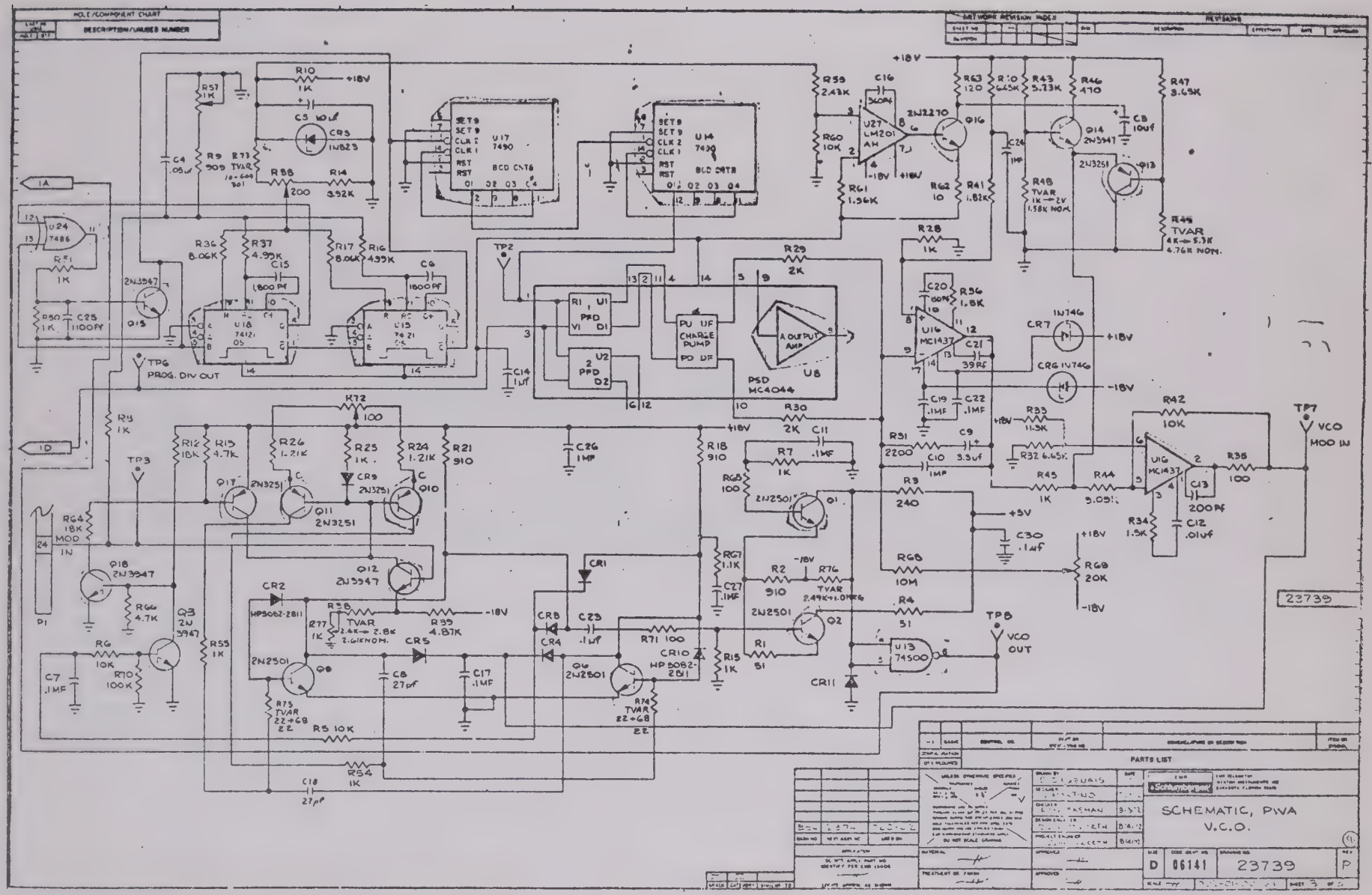


Figure 5-20 (Sheet 3 of 3). VCO PWA (Card 6) Schematic Diagram

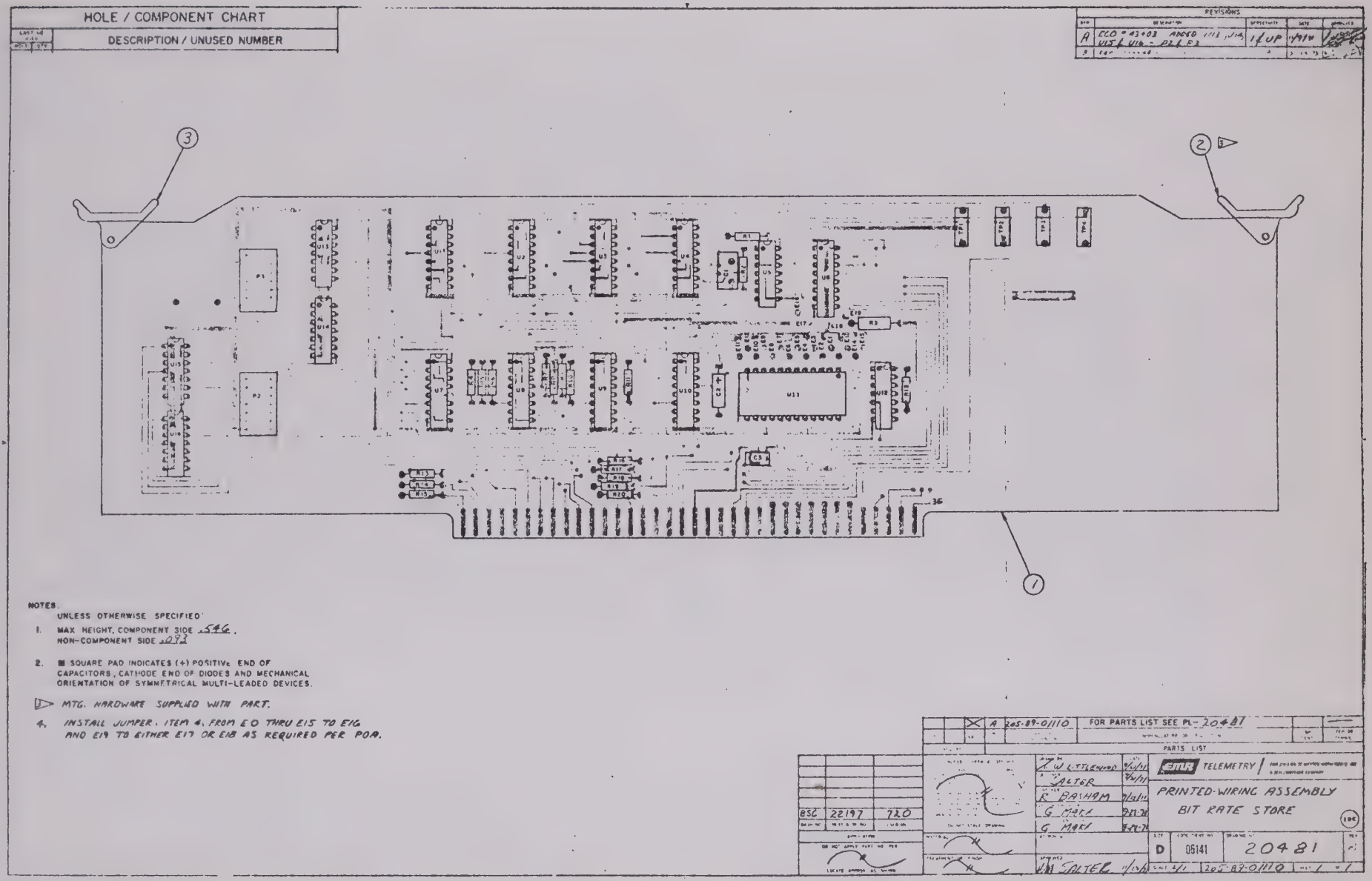


Figure 5-21. Bit Rate Store PWA (Card 7) Diagram

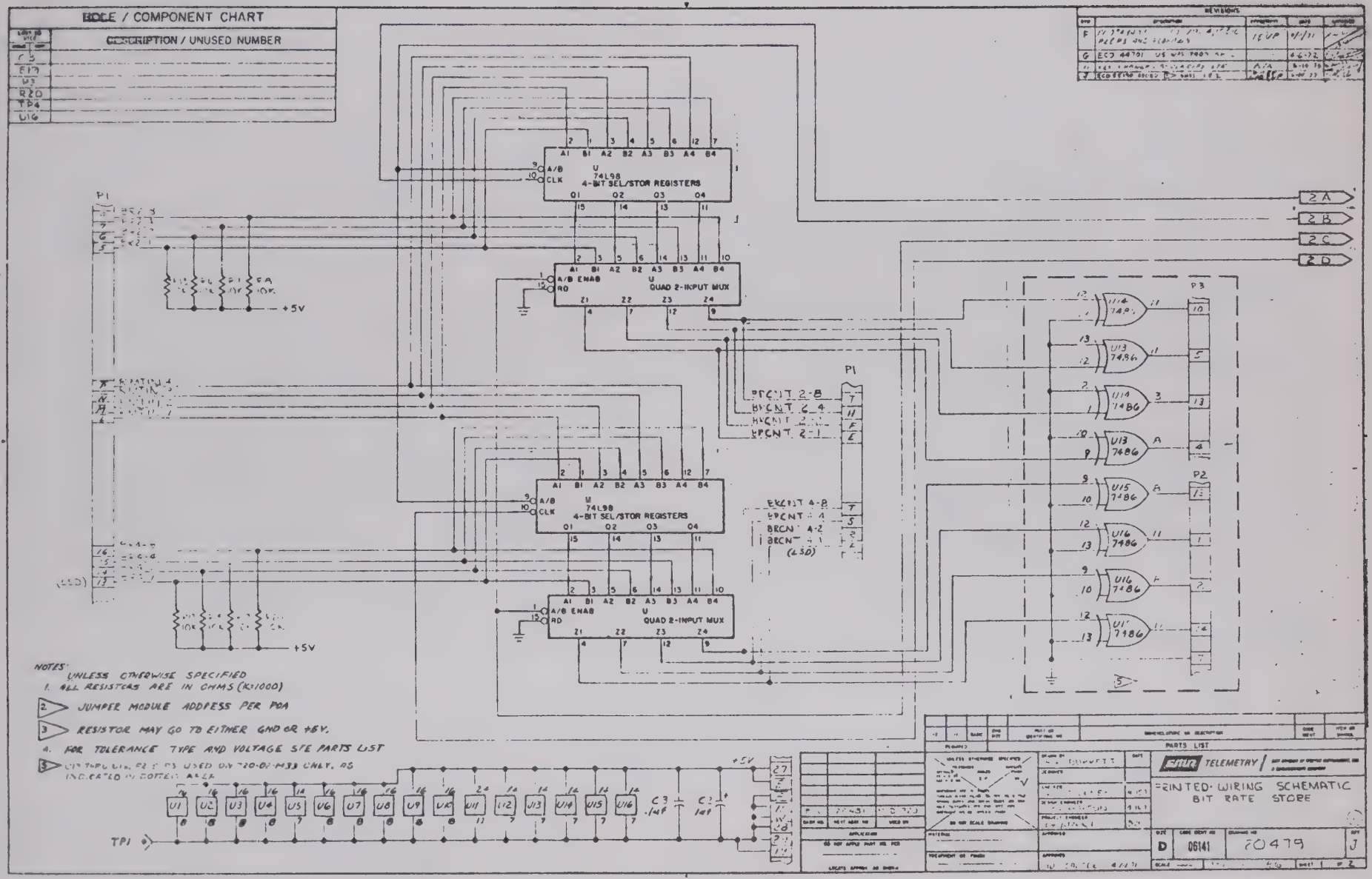


Figure 5-22 (Sheet 1 of 2). Bit Rate Store (Card 7) Schematic Diagram

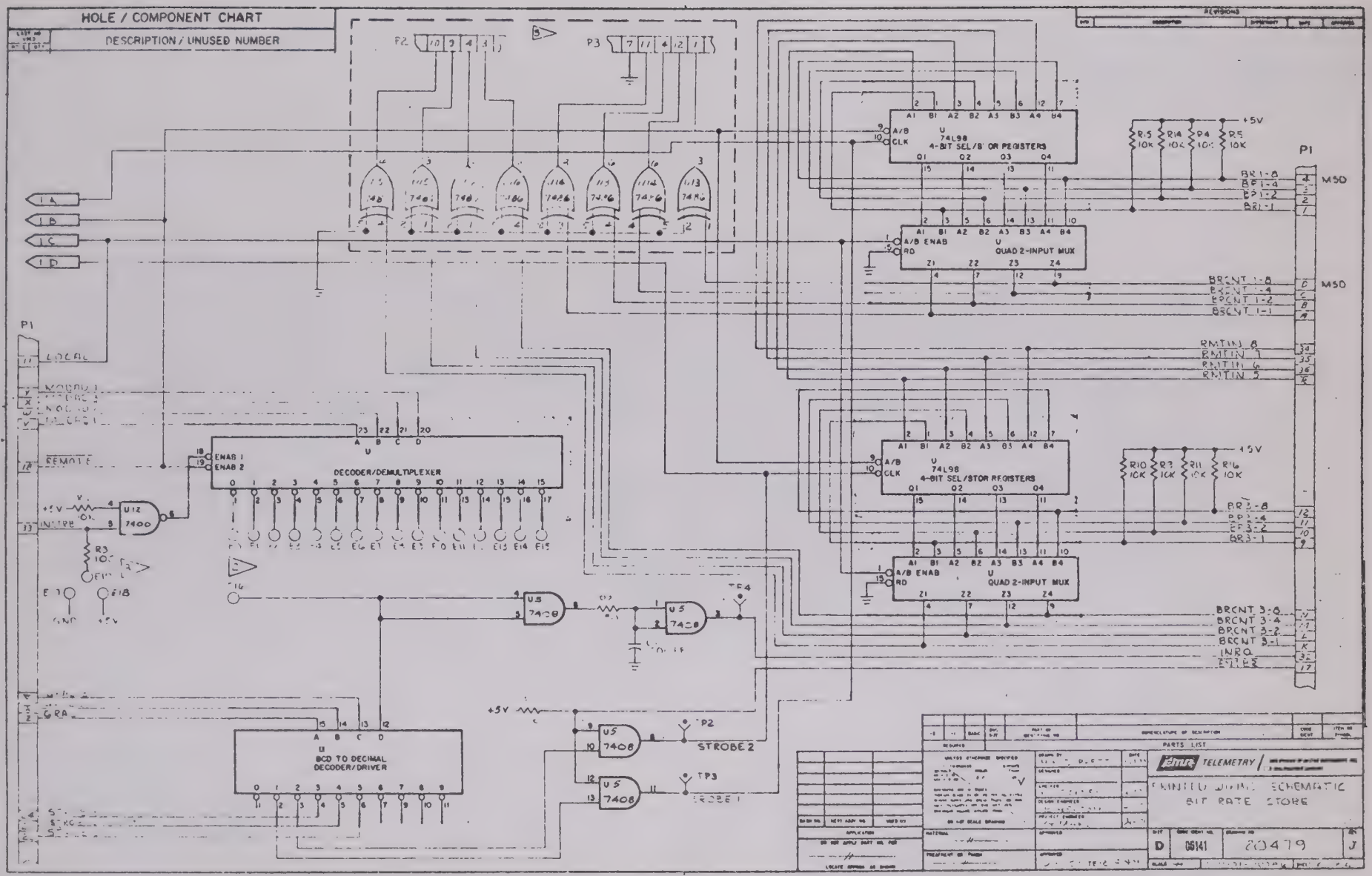


Figure 5-22 (sheet 2 of 2). Bit Rate Store (Card 7) Schematic Diagram

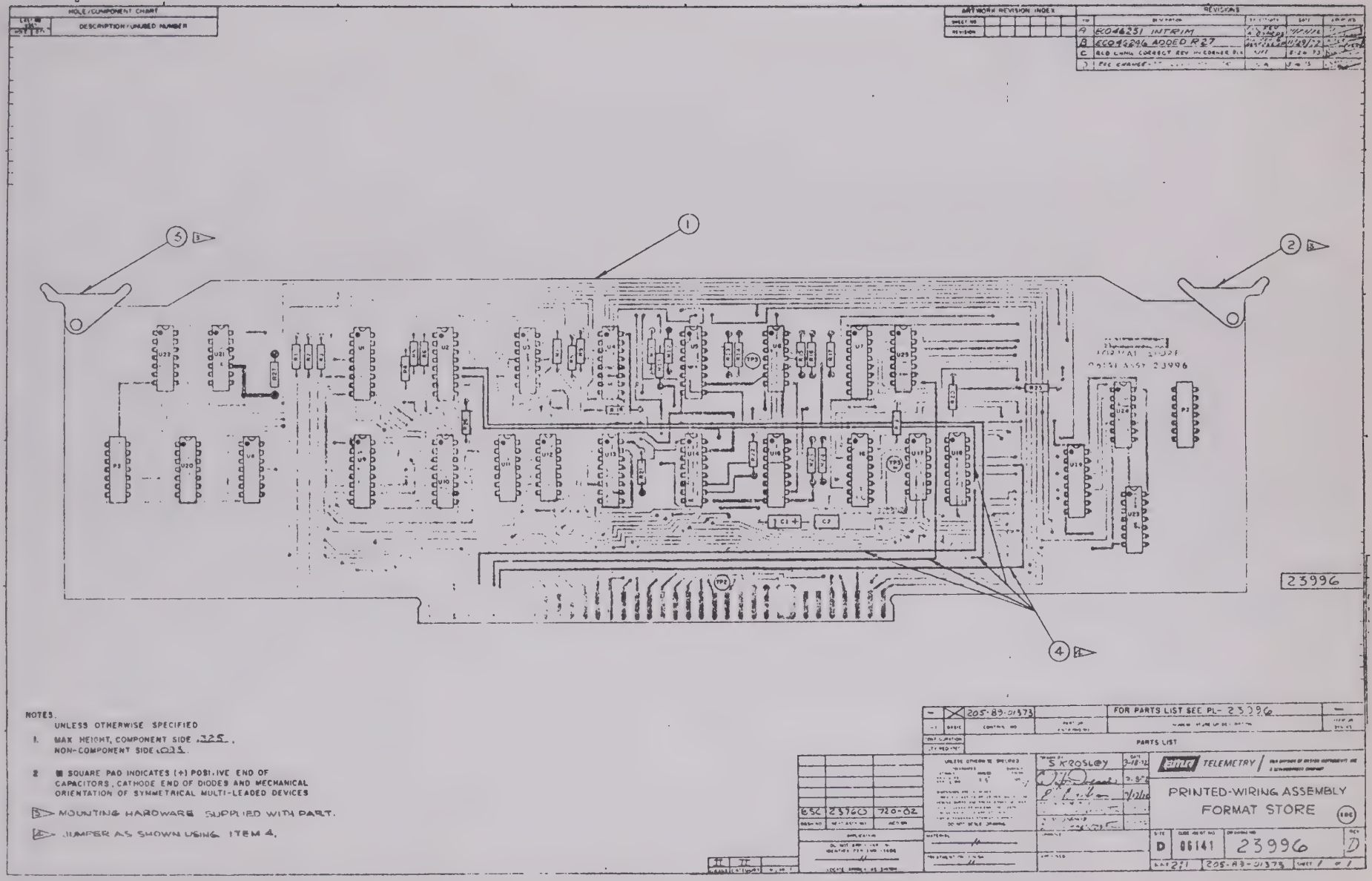


Figure 5-23. Format Store PWA (Card 8) Diagram

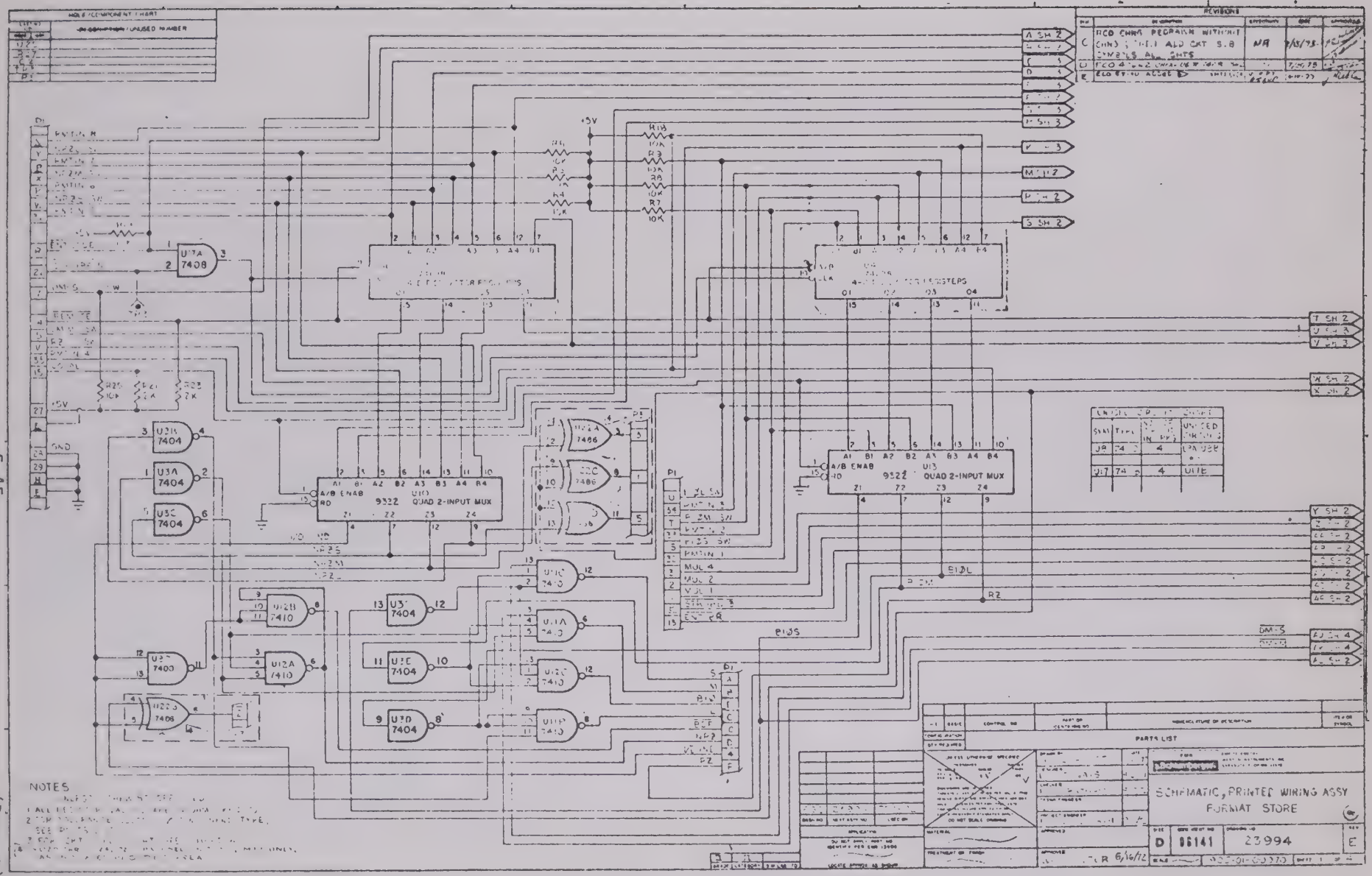


Figure 5-24 (Sheet 1 of 4). Format Store PWA (Card 8) Schematic Diagram

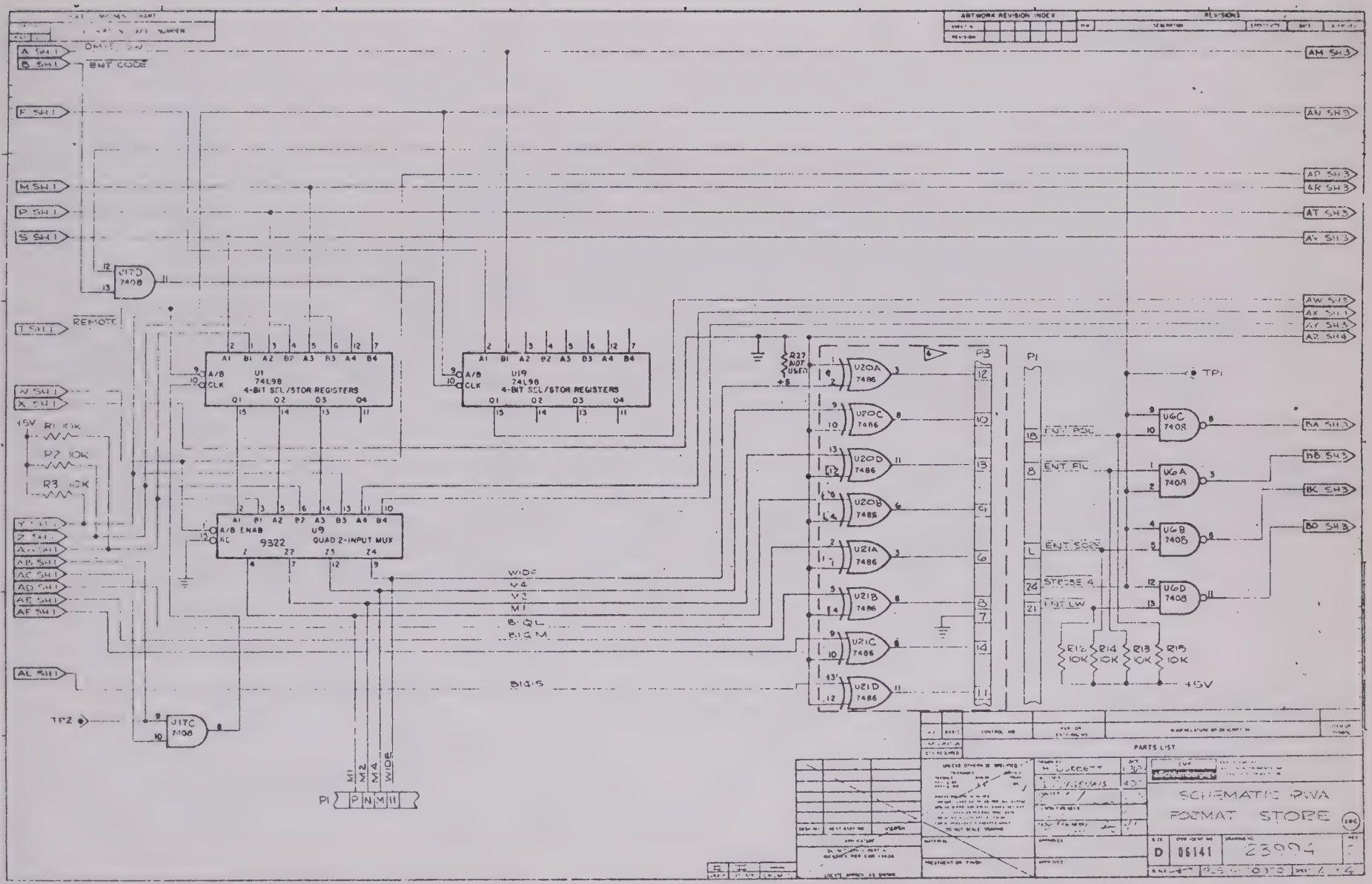


Figure 5-24 (Sheet 2 of 4). Format Store PWA (Card 8) Schematic Diagram

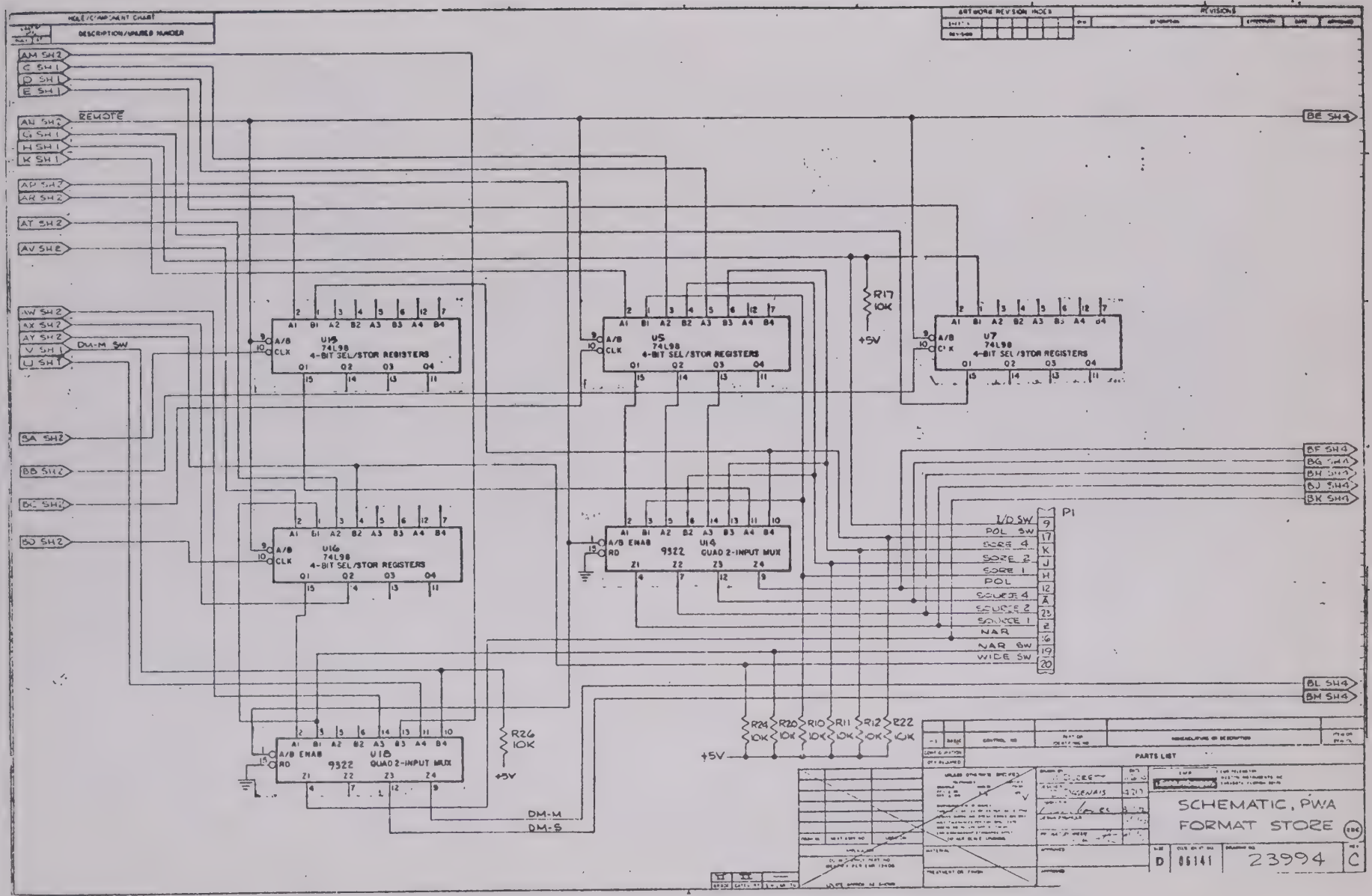


Figure 5-24 (Sheet 3 of 4). Format Store PWA (Card 8) Schematic Diagram

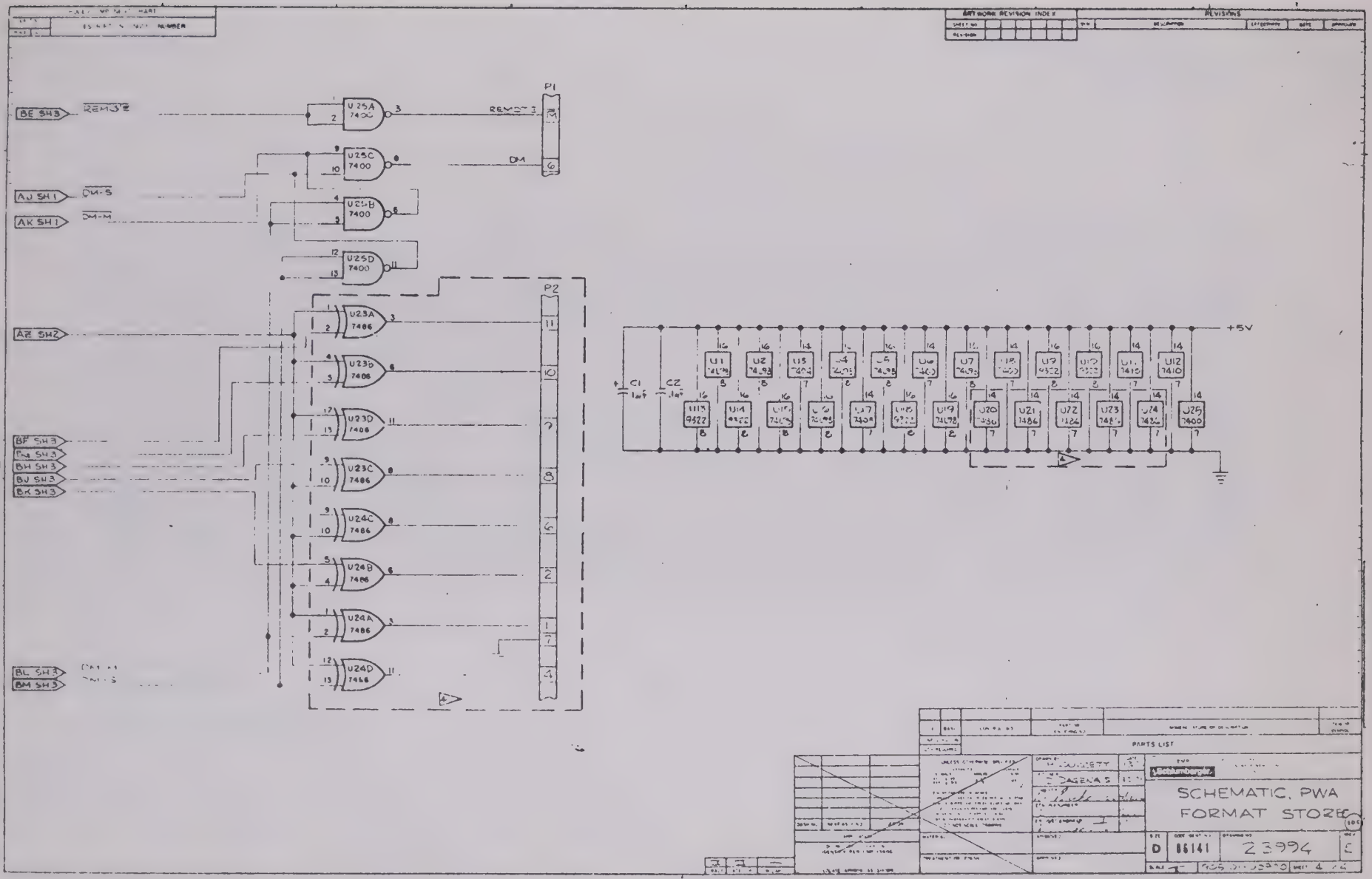


Figure 5-24 (Sheet 4 of 4). Format Store PWA (Card 8) Schematic Diagram

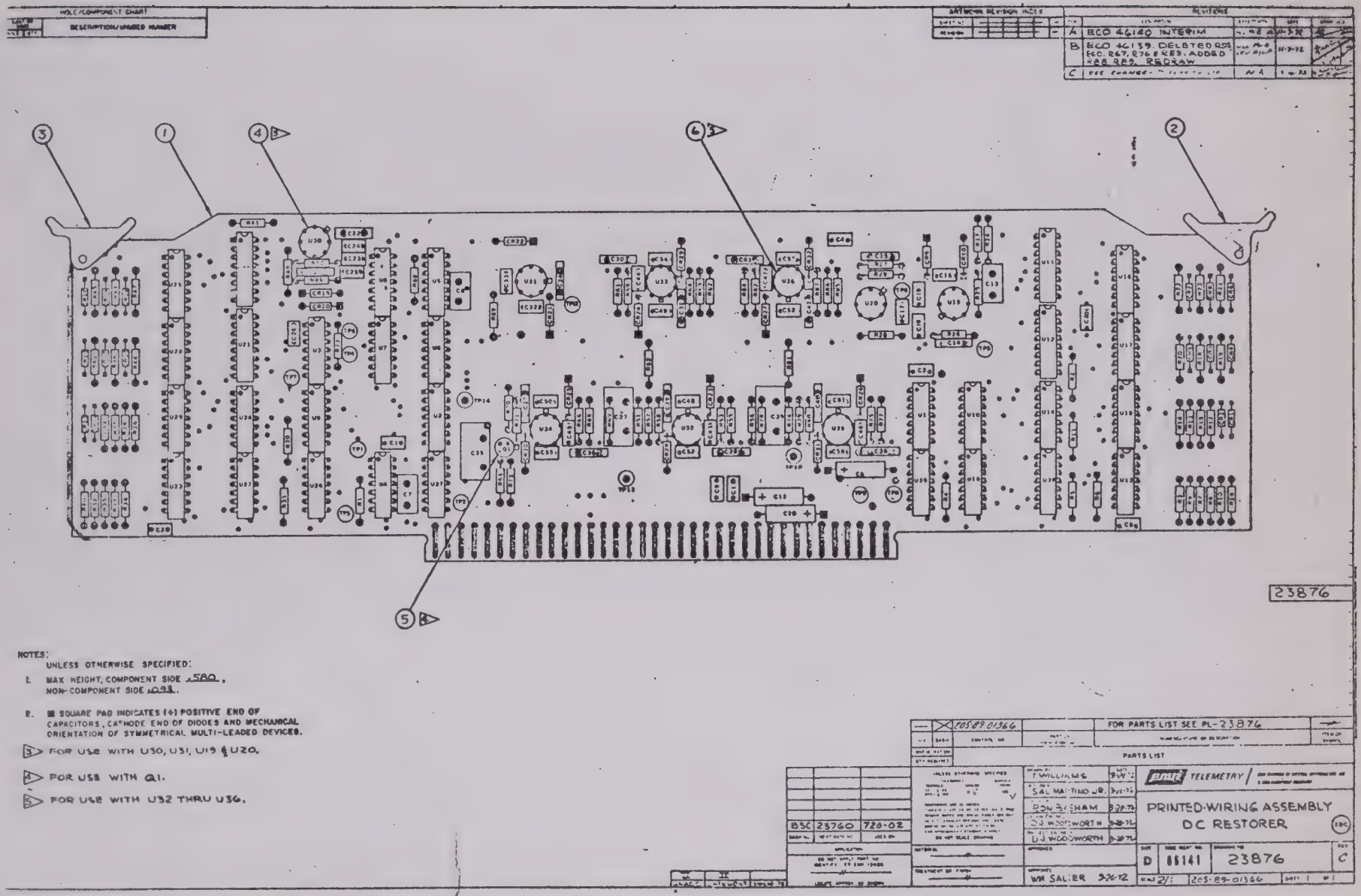


Figure 5-25. DC Restorer PWA (Card 9) Diagram

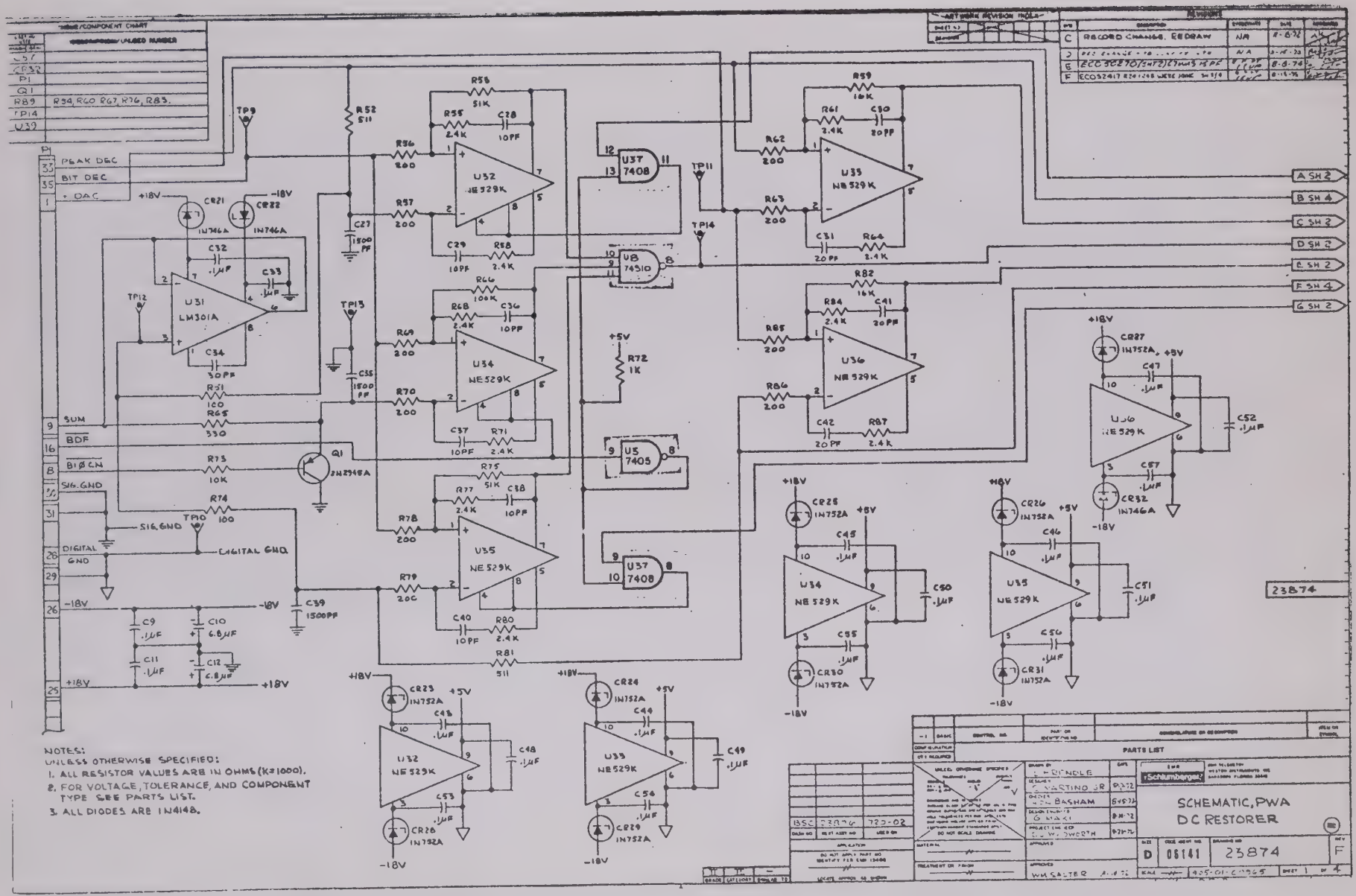


Figure 5-26 (Sheet 1 of 4). DC Restorer PWA (Card 9) Schematic Diagram

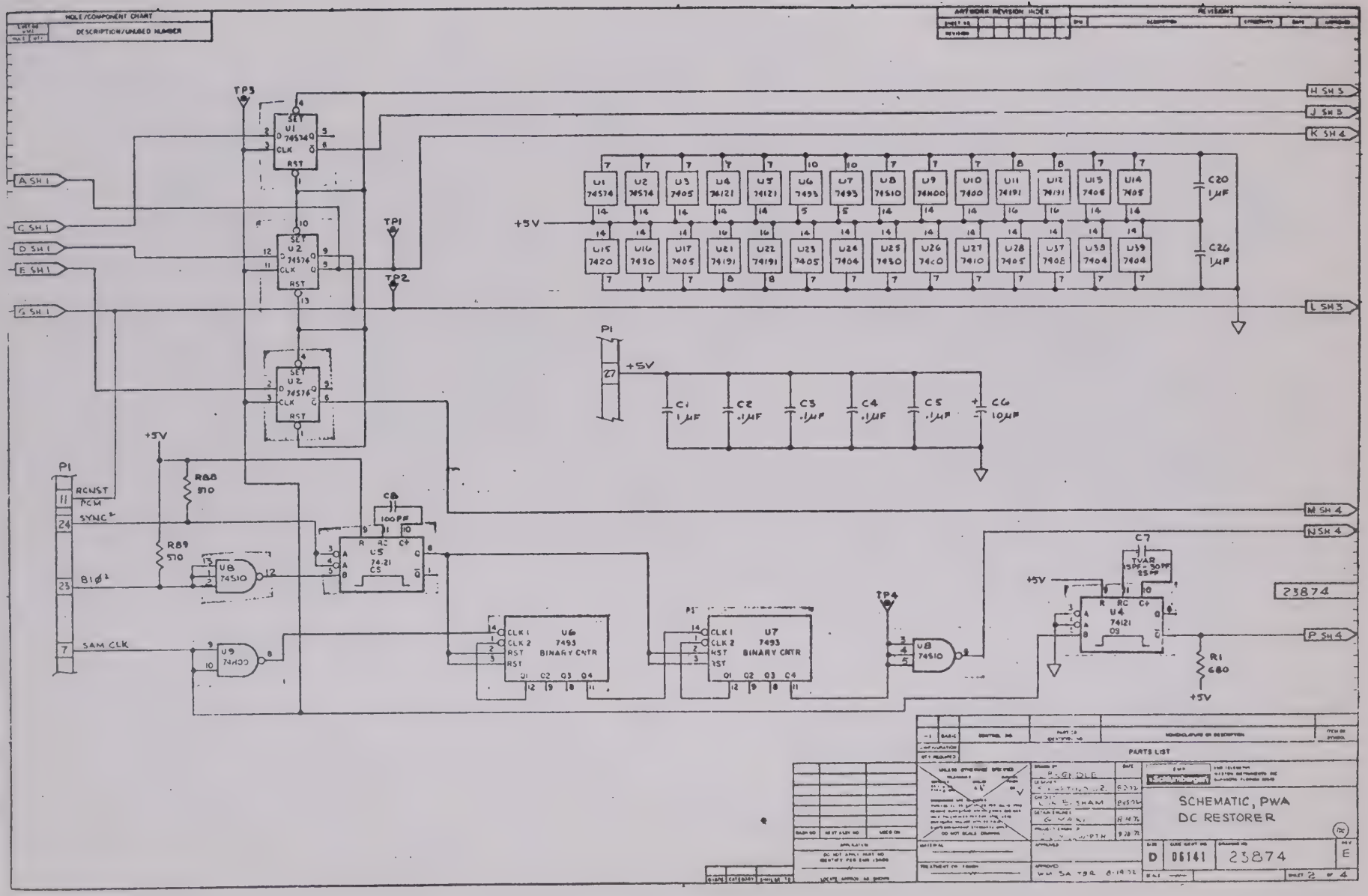


Figure 5-26 (Sheet 2 of 4). DC Restorer PWA (Card 9) Schematic Diagram

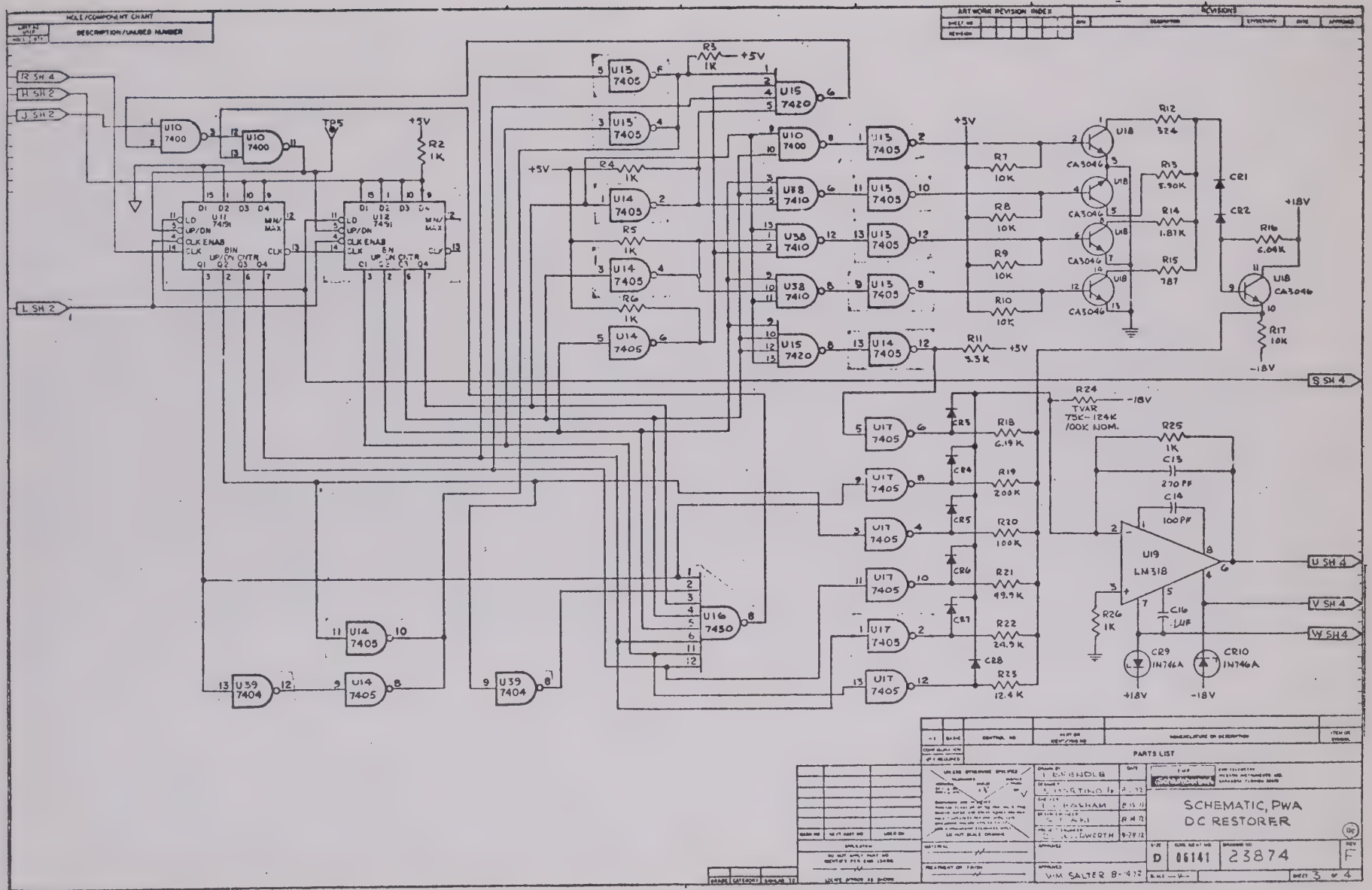


Figure 5-26 (Sheet 3 of 4). DC Restorer PWA (Card 9) Schematic Diagram

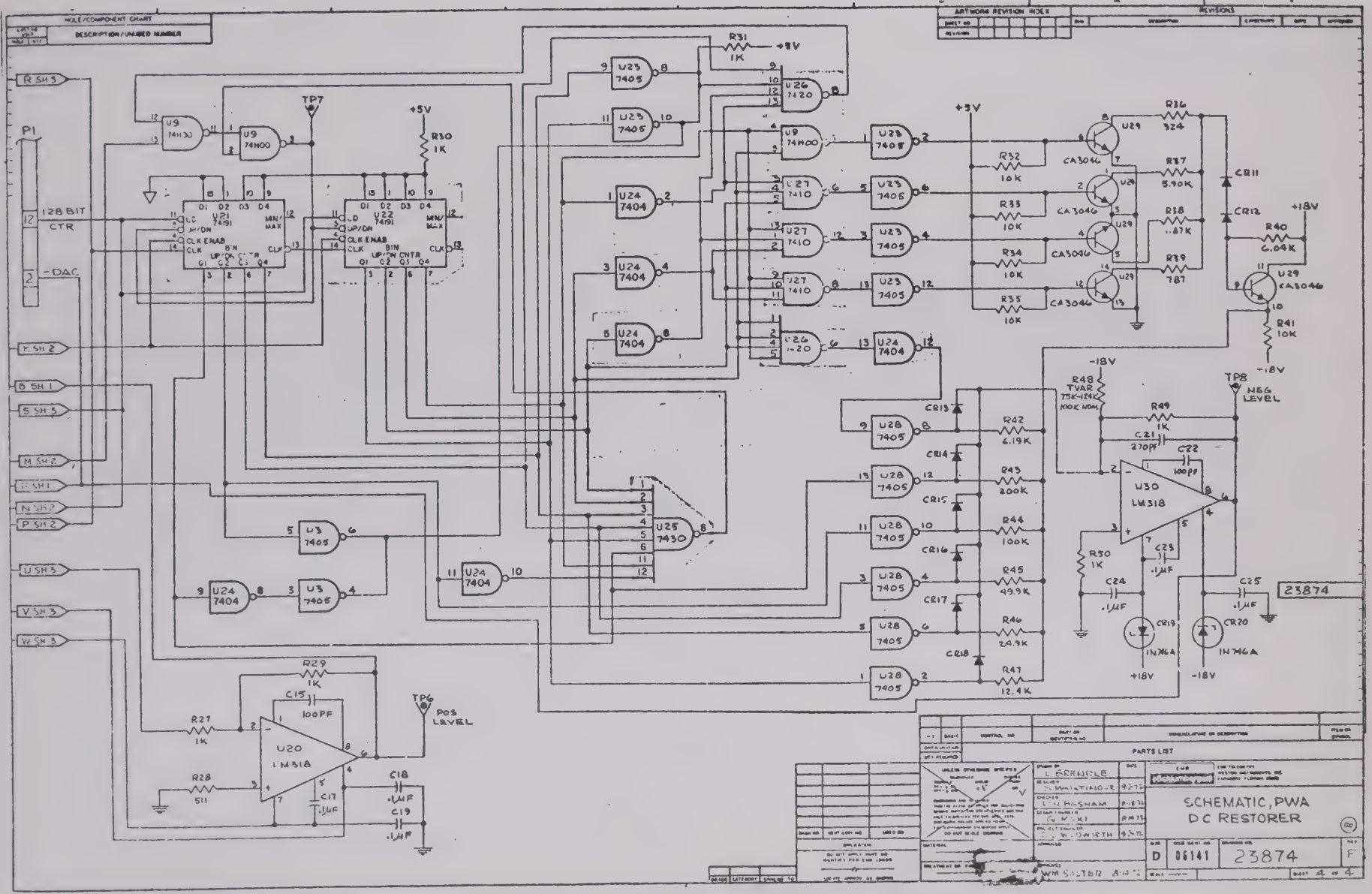


Figure 5-26 (Sheet 4 of 4). DC Restorer PWA (Card9) Schematic Diagram

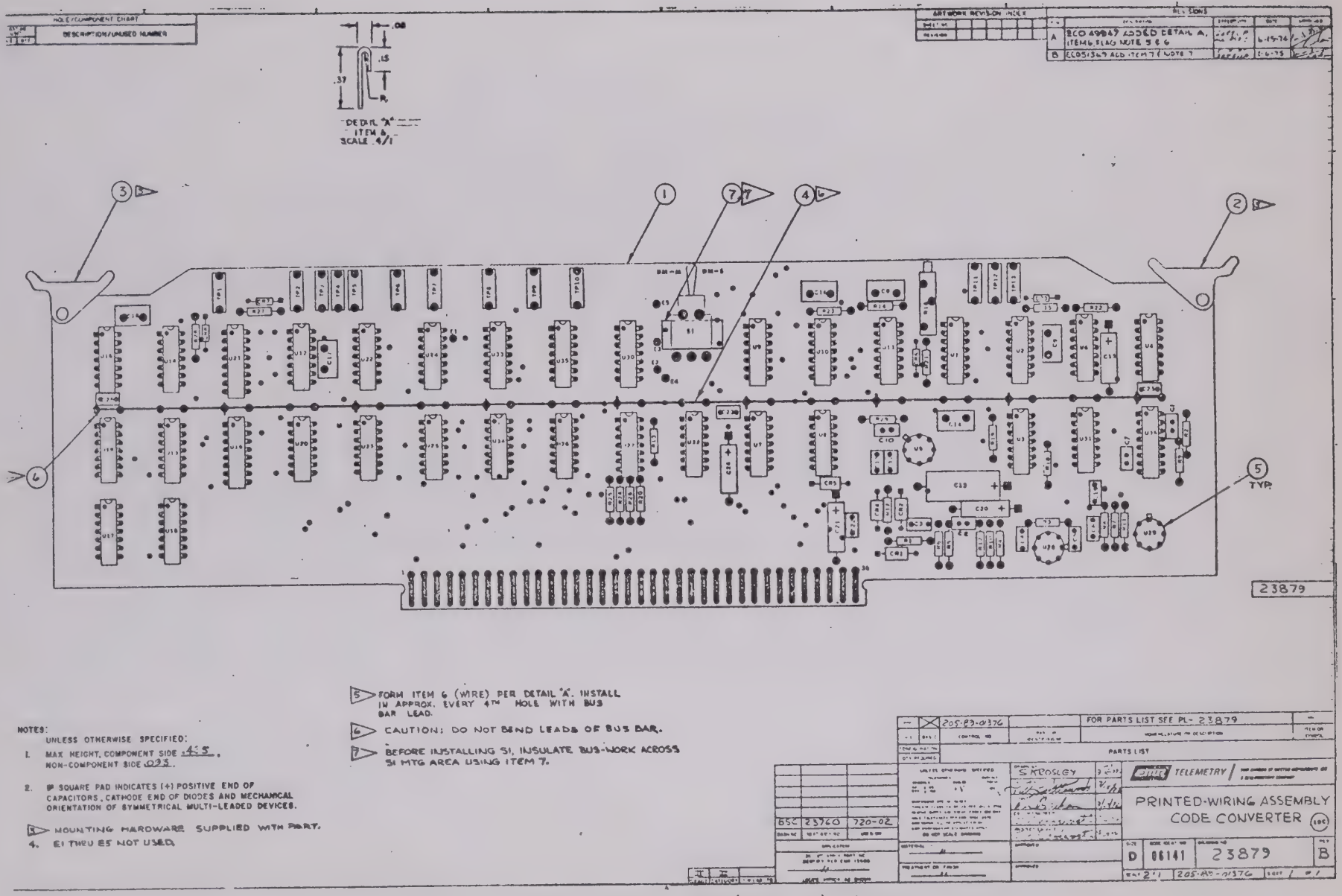


Figure 5-27. Code Converter PWA (Card 10) Diagram

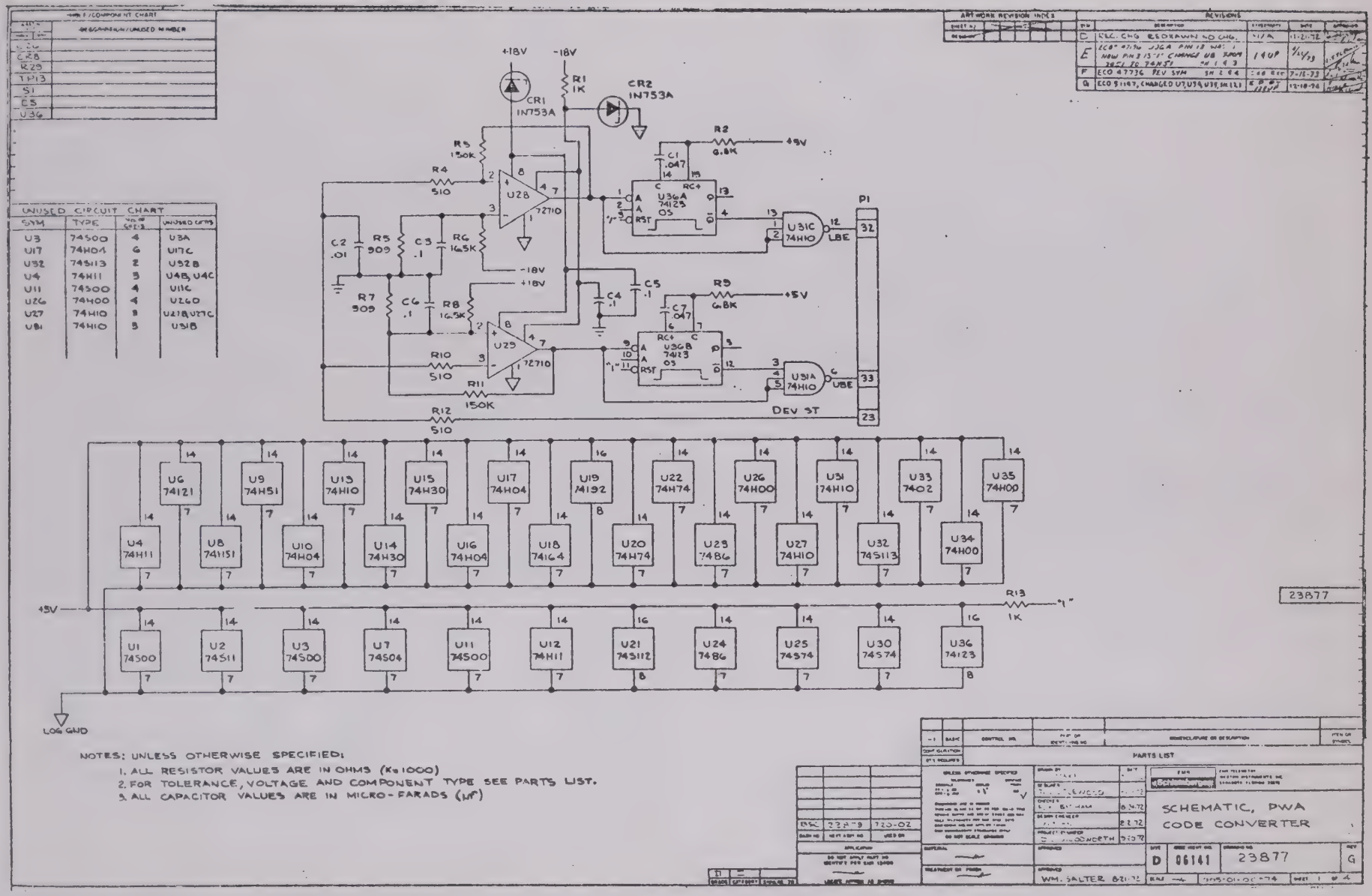


Figure 5-28 (Sheet 1 of 4). Code Converter PWA (Card 10) Schematic Diagram

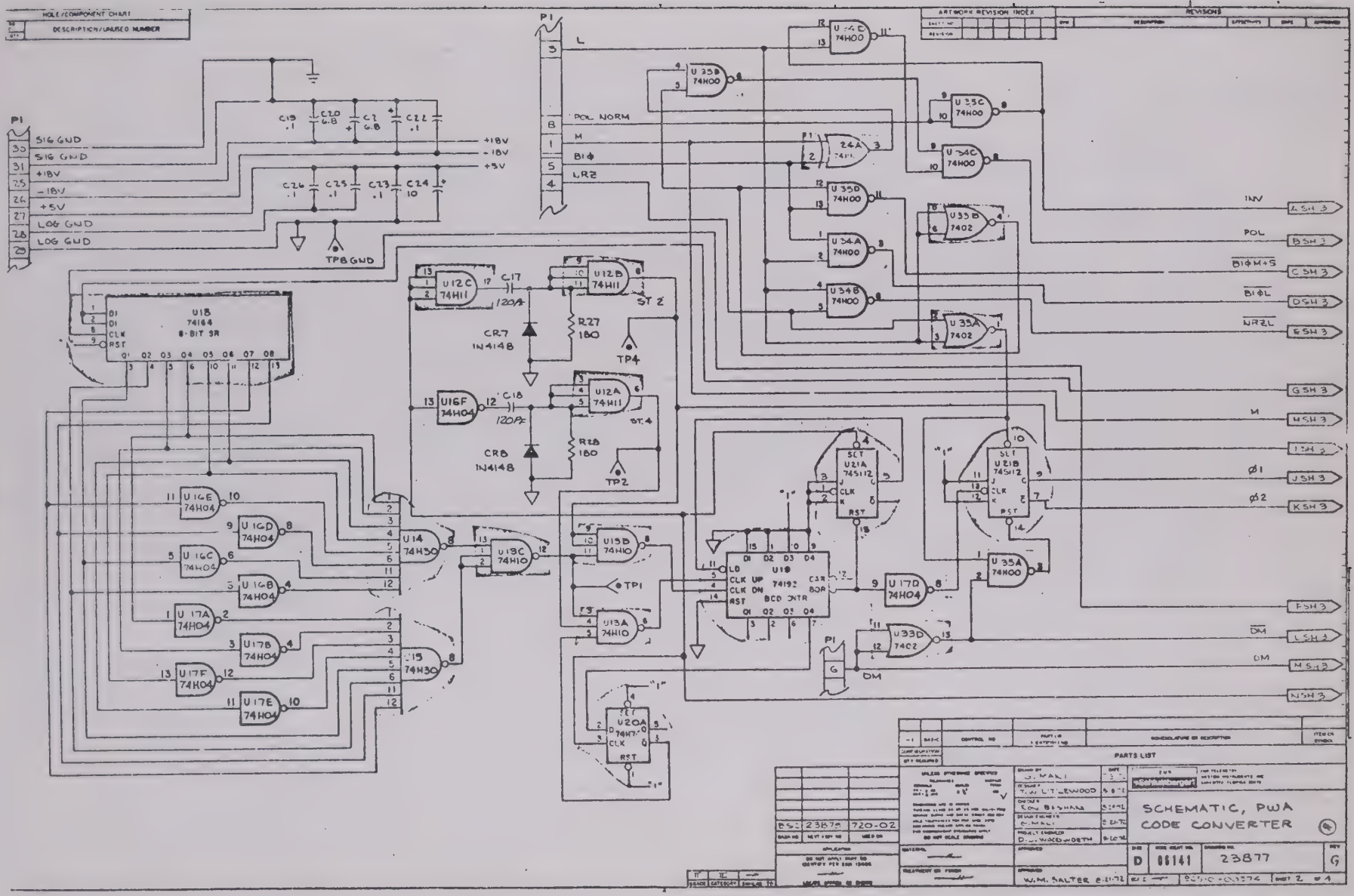


Figure 5-28 (Sheet 2 of 4). Code Converter PWA (Card 10) Schematic Diagram

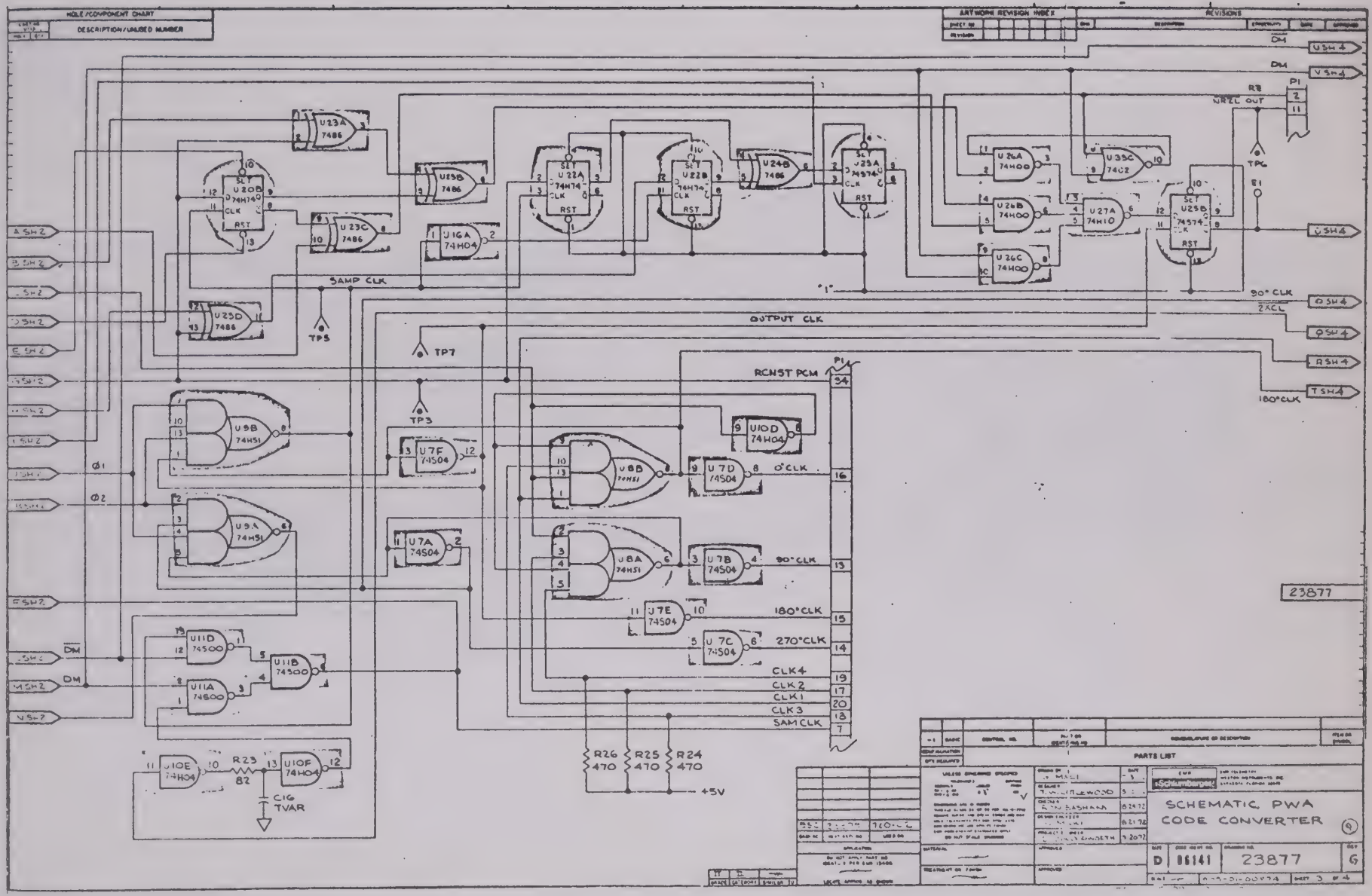


Figure 5-28 (Sheet 3 of 4). Code Converter PWA (Card 10) Schematic Diagram

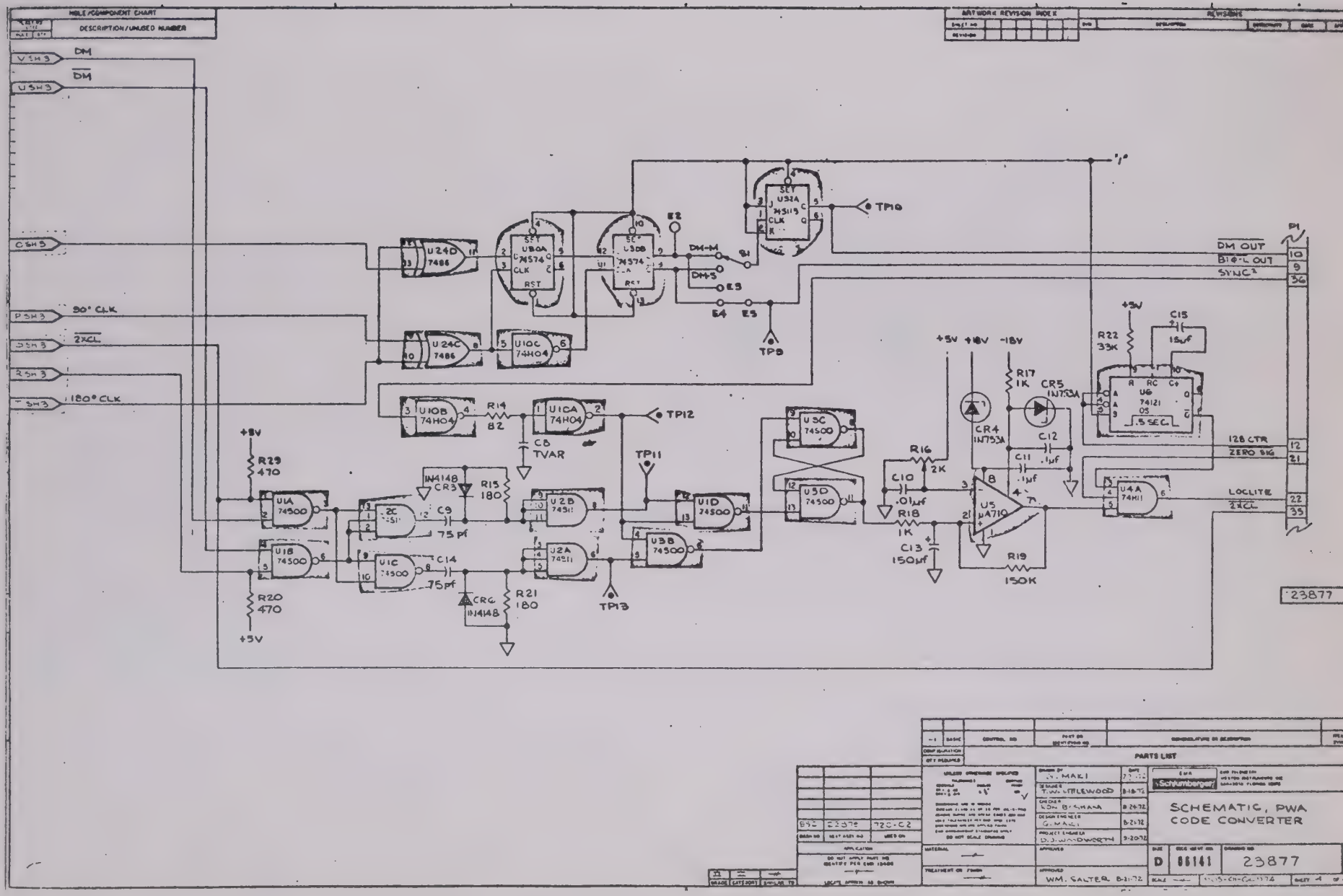


Figure 5-28 (Sheet 4 of 4). Code Converter PWA (Card 10) Schematic Diagram

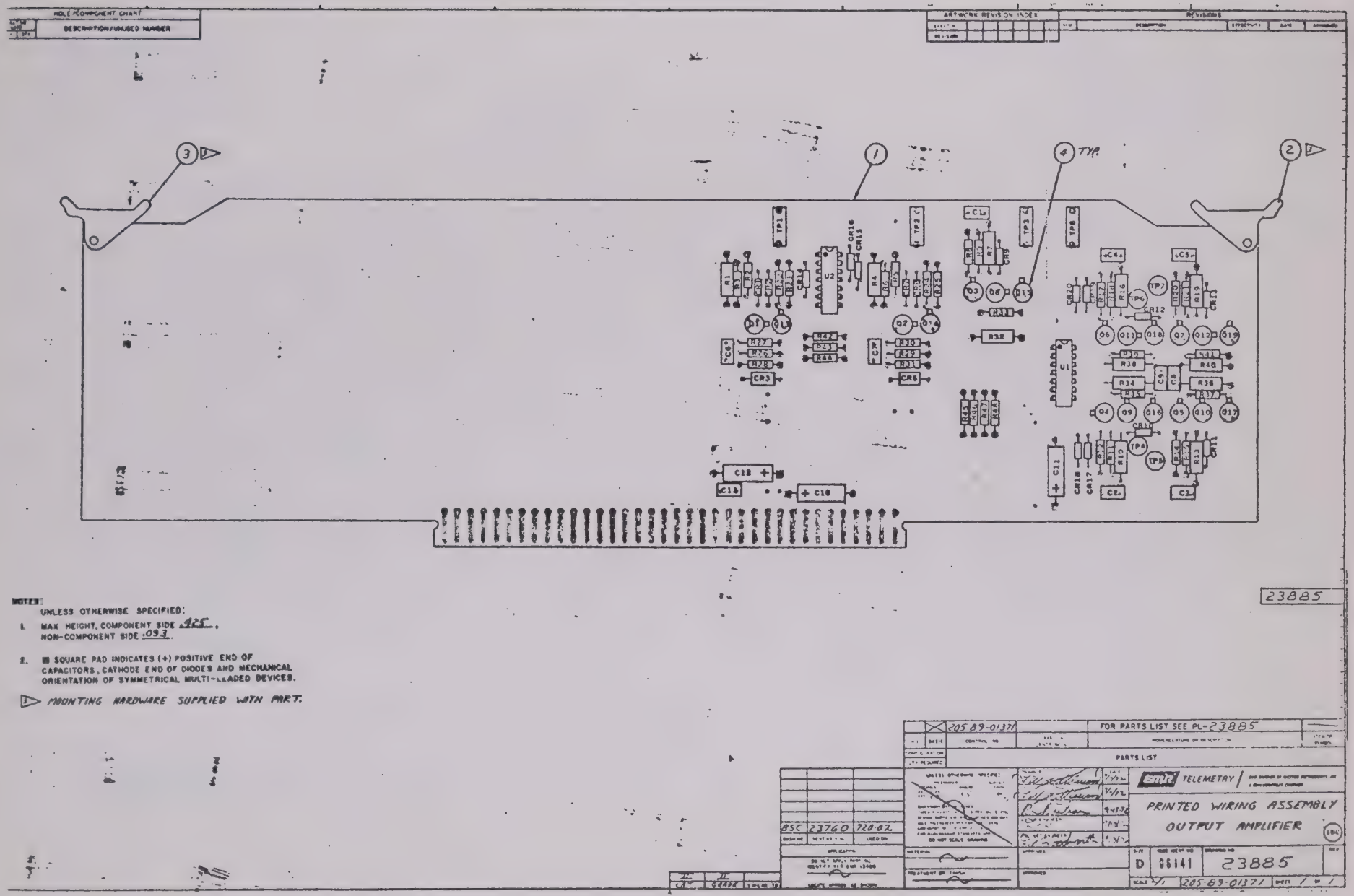


Figure 5-29. Output Amplifier PWA (Card 11) Diagram

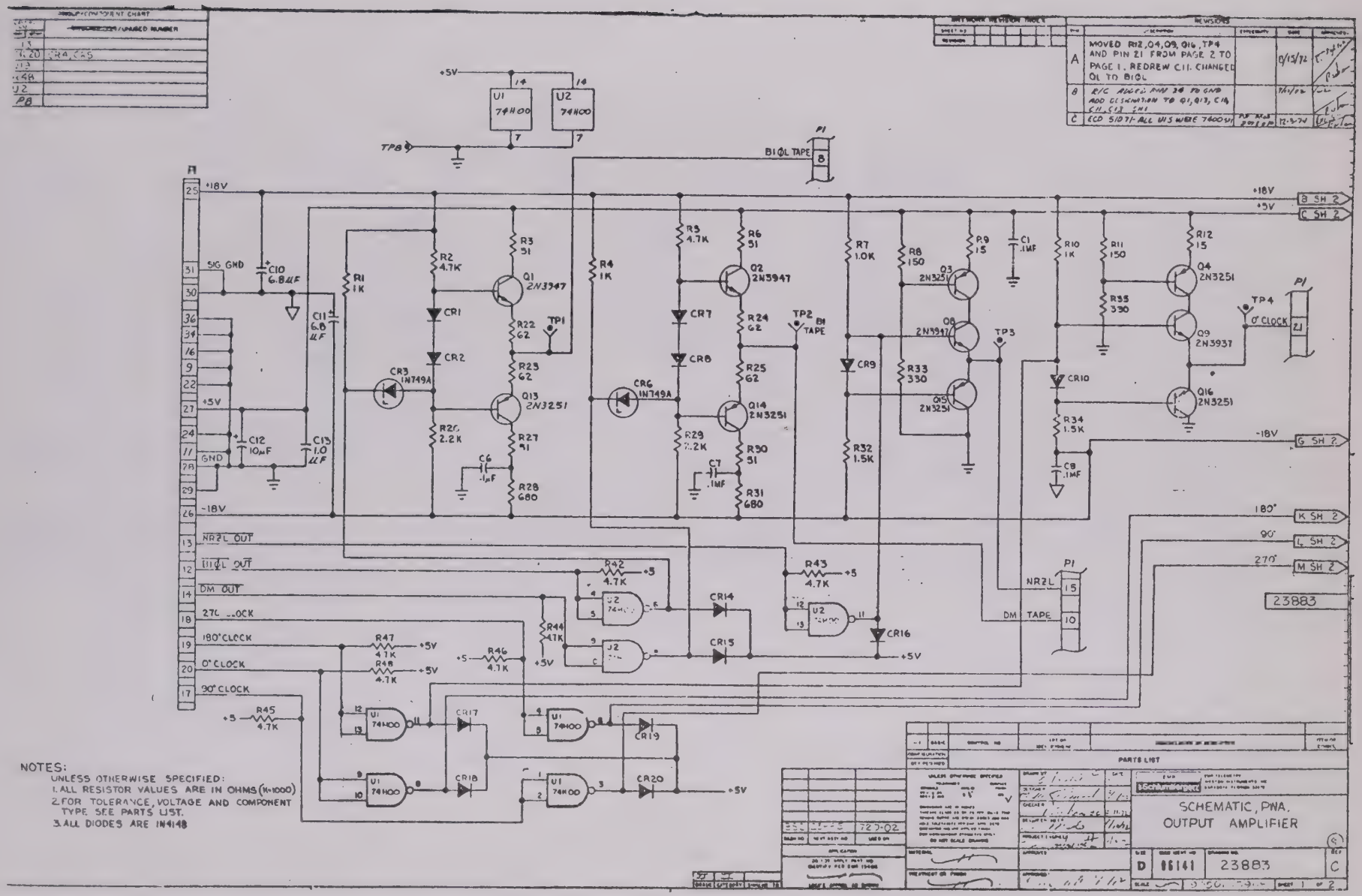


Figure 5-30 (Sheet 1 of 2). Output Amplifier PWA (Card 11) Schematic Diagram

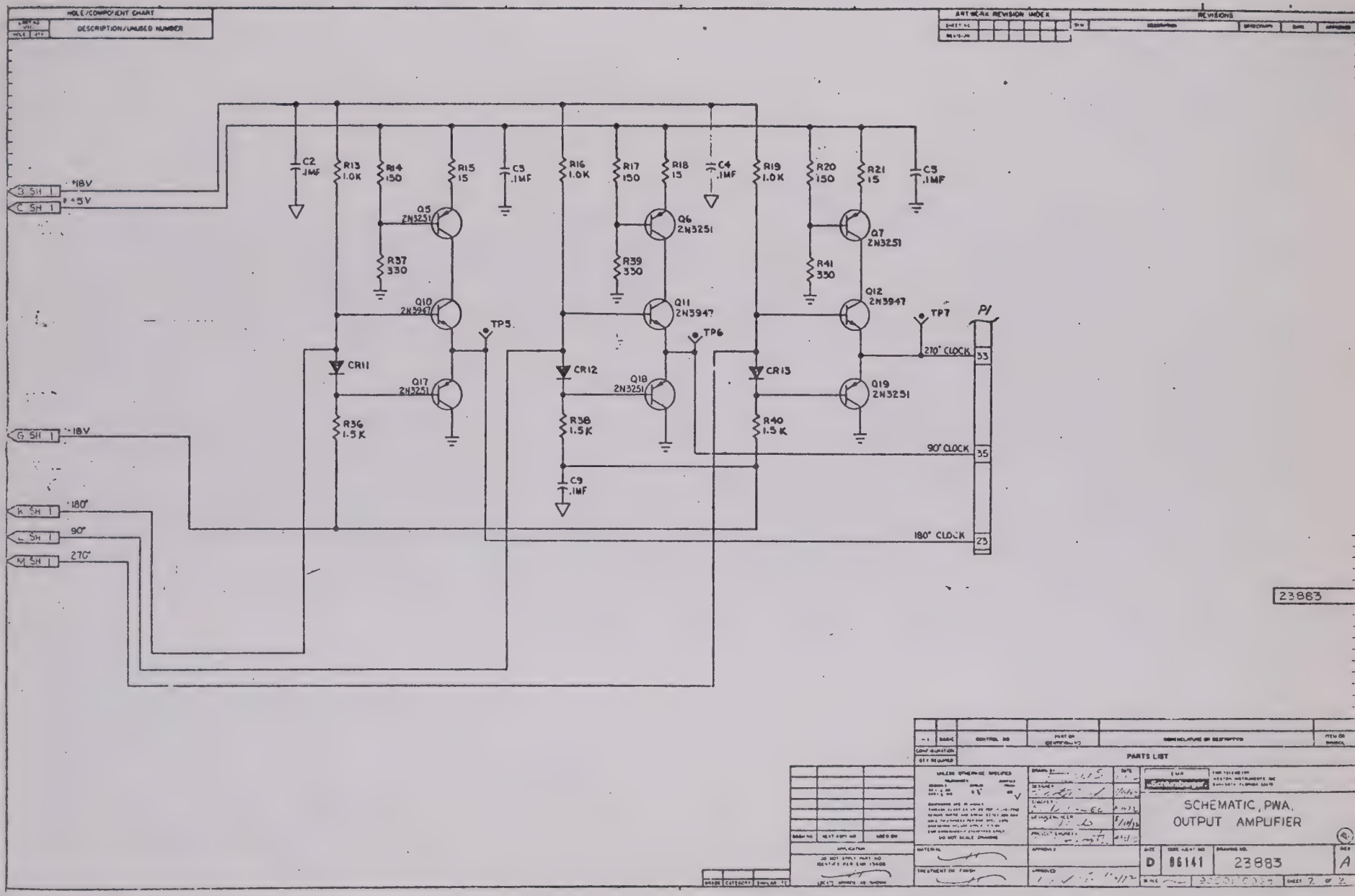


Figure 5-30 (Sheet 2 of 2). Output Amplifier PWA (Card 11) Schematic Diagram

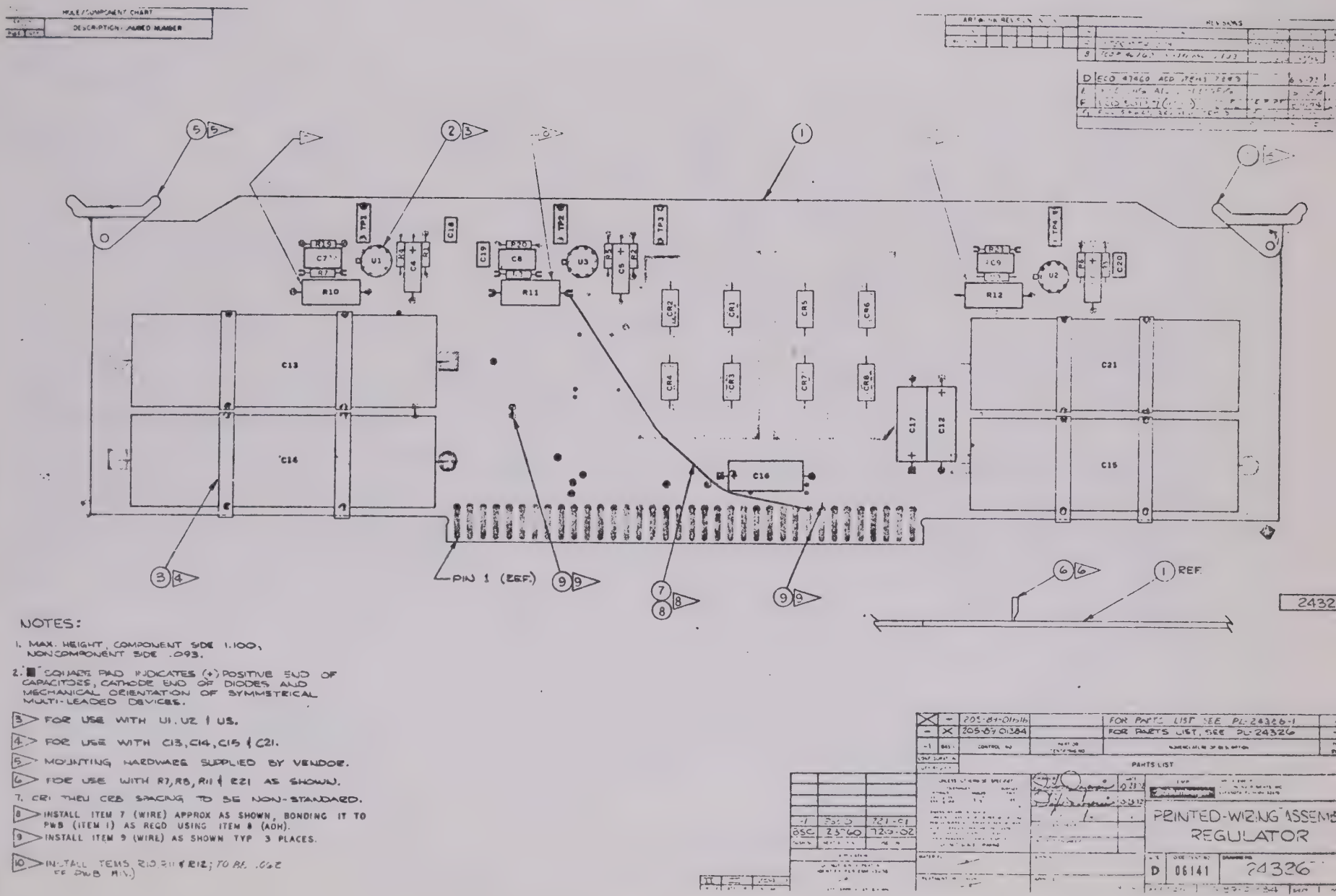


Figure 5-31. Regulator PWA (Card 13) Diagram

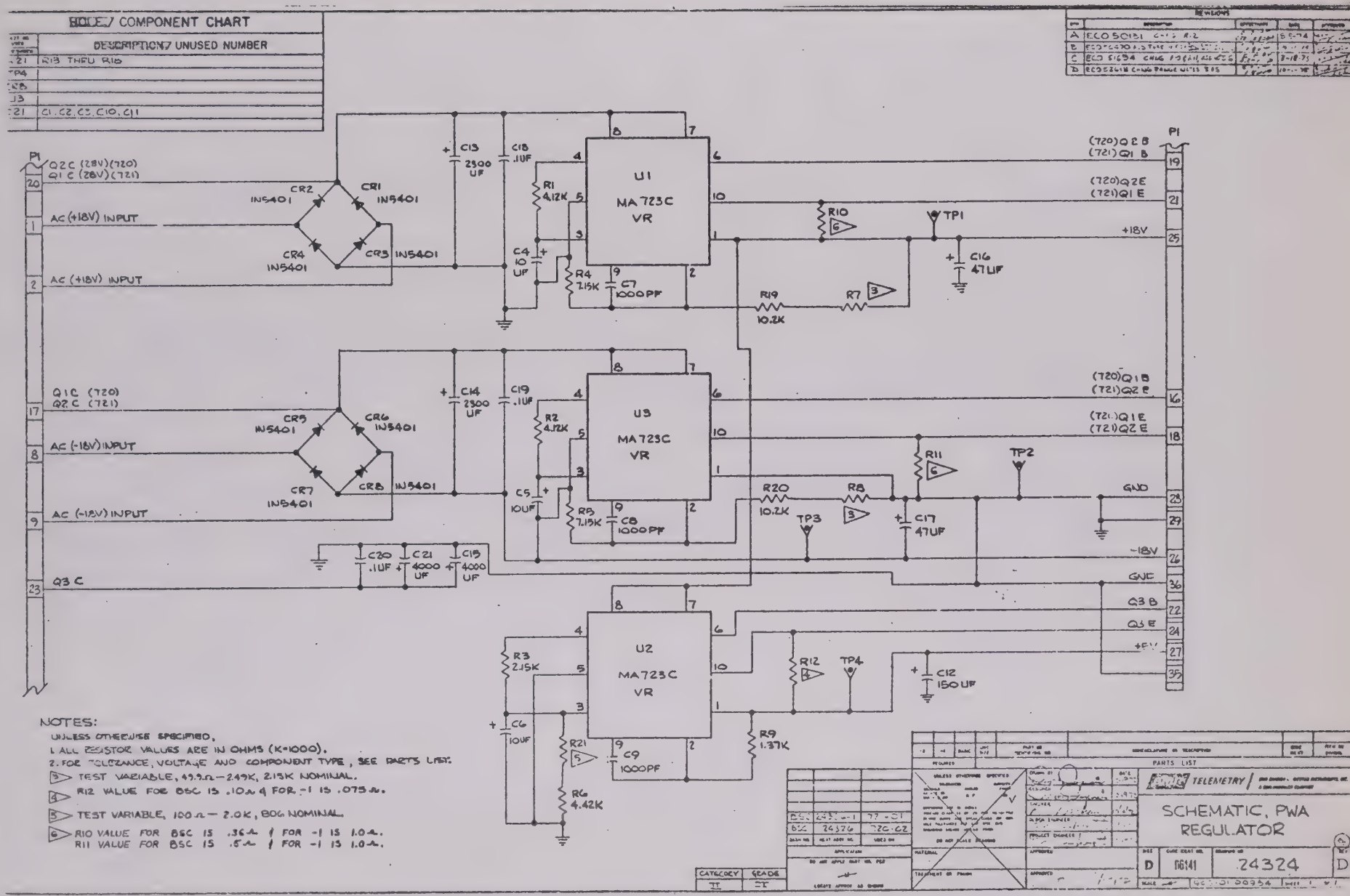


Figure 5-32. Regulator PWA (Card 13) Schematic Diagram

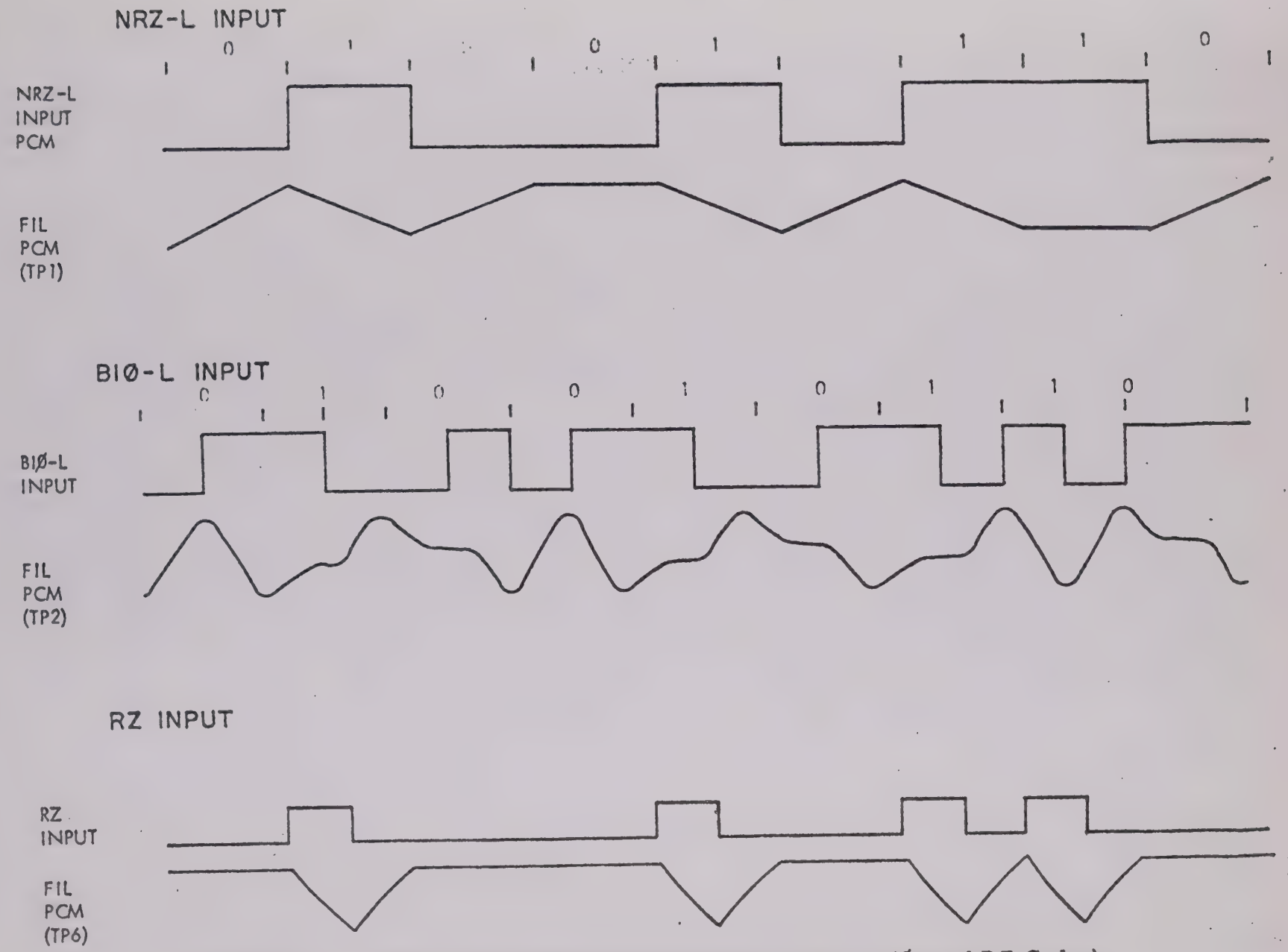


Figure 5-33. Filter Input/Output Waveforms (For NRZL, BiØ, and RZ Codes)

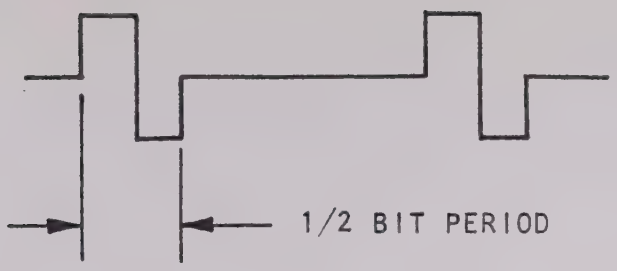


Figure 5-34. Tri-Level Pulse Train
(For NRZ Codes At BR <1 Mbps)

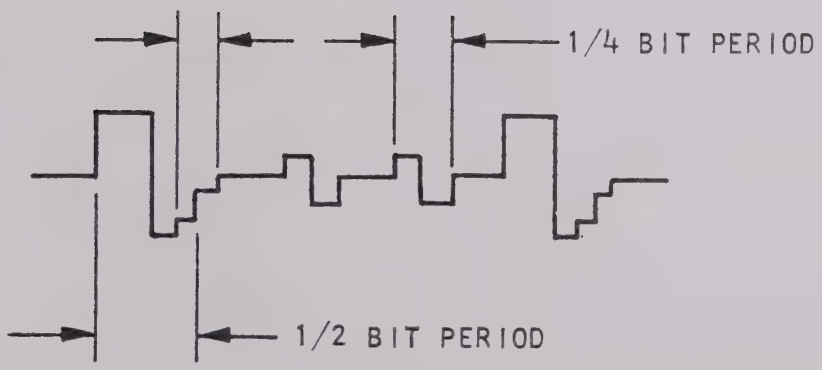


Figure 5-35. Tri-Level Pulse Train
(For BiØ Codes)

PARTS LIST

SECTION 6

PARTS LISTS AND RECOMMENDED SPARES

6.1 GENERAL

This section contains information concerning parts replacement, spares provisioning, and parts ordering information for the EMR Model 720 Bit Synchronizer. Paragraph 6.2 describes the parts breakdown for the unit as provided in this manual. Recommended spares, spares provisioning information, and parts ordering instructions are contained in paragraphs 6.3 and 6.4, respectively.

6.2 PARTS LIST DESCRIPTION

Table 6-1 identifies the individual parts lists provided in this section for the 720 and references the appropriate assembly diagram for each list. Parts List PL28370 contains the top-level parts breakdown for the Model 720. This breakdown lists all components mounted directly to the chassis of the Model 720 and its individual subassemblies. Subsequent parts lists, as identified in Table 6-1, provide detailed component breakdowns of the subassemblies.

The parts list for each assembly contains a listing of all subassemblies and components of the assembly. These subassemblies and/or components are identified by an item number in the ITEM NO. column. The ITEM NO. (or component designation) corresponds to numbers in the reference balloons on the associated EMR drawing. Also included in the parts list for each item are the quantity required (QTY REQ'D), EMR PART NUMBER, EMR DRAWING or SPEC NO., item DESCRIPTION, VENDOR NAME AND VENDOR PART NUMBER.

6.3 RECOMMENDED SPARES

A list of the recommended spare parts for the Model 720 is contained in Table 6-2. The recommended spares as listed in this table are based on the following conditions:

a. Operating time -- 8 hours/day, 5 days/week (2080 hours/year).

b. Operating Temperature -- 0° C to 50° C.

c. User has capability to repair to the component level.

d. Failure rates are constant.

e. 0.9 probability of being able to repair from the recommended complement for one year.

f. Equipment will be used as ground equipment (as opposed to vehicular or airborne).

The recommended spares table contains a PART DESCRIPTION column, an EMR STOCK NO. column, a TQ column which is the total quantity of the part in the unit, and an RS column which lists the number of recommended spares for the part.

6.4 ORDERING INSTRUCTIONS

When ordering parts, EMR stock number and complete description of each part as listed in DESCRIPTION column of parts list must accompany order.

Table 6-1. Model 720-02 Parts List Identification

ITEM	PARTS LIST NO.	FIGURE NO.
Bit Synchronizer Assembly	28370	5-1
Interconnection Board A1	24023	5-3
Front Panel Assembly A2	28276	5-5
Rear Panel Assembly A4	33871	5-7
Heatsink Assembly (Mounted on Right Side Panel Assembly A3)	21819-2	5-8
Source Select Printed-Wiring Assembly (Card 1)	20457	5-9
Input Filter Printed-Wiring Assembly (Card 2) (1st Pole)	23738	5-11
Input Filter Printed-Wiring Assembly (Card 3) (2nd Pole)	23745	5-13
Filter Control Assembly (Card 4)	24005	5-15
Loop Filter Printed-Wiring Assembly (Card 5)	24019	5-17
VCO Printed-Wiring Assembly (Card 6)	23741	5-19
Bit Rate Store Printed-Wiring Assembly (Card 7)	20481	5-21
Format Store Printed-Wiring Assembly (Card 8)	23996	5-23
DC Restorer Printed-Wiring Assembly (Card 9)	23876	5-25
Code Converter Printed-Wiring Assembly (Card 10)	23879	5-27
Output Amplifier (Card 11)	23885	5-29
Regulator Printed-Wiring Assembly (Card 13)	24326	5-31

720-02 PARTS LISTS

The parts lists appear in the order listed in Table 6-1.

E M R - T E L E M E T R Y

PARTS LIST 28370 REV DATE 01/09/78 REV LTR P

LIST TITLE SYNCH,PCM BIT,ASSY CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 407-89-00326 ECO 55708 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	2	400-89-C0007	25122-1	FRAME,ASSY,BEZEL	EMR	400-89-00007	
2	2	200-99-00010	25207-1	POST,CORNER,FRONT	EMR	200-99-00010	
3	2	200-99-00017	25208-1	POST,CORNER,REAR	EMR	200-99-00017	
4	1	016-89-C0129	24569-2	BRKT,ASSY,RS,RACK MOUNT	EMR	016-89-00129	
5	1	016-89-00130	24569-3	BRKT,ASSY,LS,RACK MOUNT	EMR	016-89-00130	
6	2	075-89-00081	24600	COVER,TOP/BOTTOM,ASSY	EMR	075-89-00081	
7	1	999-01-00004	28376	PANEL, SIDE, *POA VAR*			
8	1	191-89-00613	28372	PANEL,SIDE,L.H.,ASSY	EMR	191-89-00613	
9	1	191-99-00549	27466	PANEL,FRONT	EMR	191-99-00549	
10	1	191-89-00747	33871	PANEL,ASSY,REAR	EMR	191-89-00747	
11	1	205-89-C1587	28276	PWA,SUBPANEL	EMR	205-89-01587	
13	1	999-02-00001	28376	SLIDES*POA VAR*			
14	1	999-01-00002	28376	PLATE WARNING*POA VAR*			
15	1	282-99-00075	27465	RAIL,INTERCONNECT,FRONT	EMR	282-99-00075	
16	1	282-99-00076	27463	RAIL,INTERCONNECT,REAR	EMR	282-99-00076	
17	1	205-89-01378	24023	PWA,INTERCONNECT	EMR	205-89-01378	
18	2	140-99-00152	21822	INSUL,RAIL	EMR	140-99-00152	
19	2	279-99-00095	21951	SPRT,INTCON BOARD	EMR	279-99-00095	
20	1	016-89-00147	27464	BRKT,ASSY,CARD GUIDE,FR	EMR	016-89-00147	
21	1	016-89-00146	28374	BRKT,ASSY,CARD GUIDE,REAR	EMR	016-89-00146	
22	1	223-99-00009	21722	ROD,SUPPORT	EMR	223-99-00009	
23	26	401-98-00011		GUIDE,CARD,.180THK X.469W	UNITRACK	SPC-3000	
24	1	016-99-00329	28202	BRKT,PWR SWITCH MOUNTING	EMR	016-99-00329	
25	1	196-99-00156	10663	PLATE,NAME EQUIP IDENT	EMR	196-99-00156	
26	1	239-99-00100	21968-13	SPACER,.38 X 2.75 X.37THK	EMR	239-99-00100	
27	1	298-89-00030	21819-2	HTSK,TRANSISTOR,ASSY	EMR	298-89-00030	
28	2	229-98-00120		SCREW,CAPTIVE PANEL,10-32	AMATOM	6141-SS-1032-9	
29	AR	060-11-00001		CMPD,LOCKING,FINE THREAD	LOCTITE CORP	LOCTITE GRADE A	
30	1	205-89-01104	20457	PWA,SOURCE SELECT	EMR	205-89-01104	
31	1	205-89-01362	23738	PWA,1ST FILTER POLE PAIR	EMR	205-89-01362	
32	1	205-89-01363	23745	PWA,2ND FILTER POLE PAIR	EMR	205-89-01363	
33	1	205-89-01377	24005	PWA, FILTER CONTROL	EMR	205-89-01377	
34	1	205-89-01361	24019	PWA,LOOP FILTER	EMR	205-89-01361	
35	1	205-89-01364	23741	PWA,VCO	EMR	205-89-01364	
36	1	205-89-01110	20481	PWA,BIT RATE STORE	EMR	205-89-01111	
37	1	205-89-01373	23996	PWA,FORMAT STORE	EMR	205-89-01373	
38	1	205-89-01366	23876	PWA, DC RESTORER	EMR	205-89-01366	
39	1	205-89-01371	23885	PWA,OUTPUT AMPLIFIER	EMR	205-89-01371	
40	1	205-89-01376	23879	PWA,CODE CONVERTER	EMR	205-89-01376	
41	1	205-89-01384	24326	PWA,REGULATOR	EMR	205-89-01384	
42	1	205-89-00501	14199	PWA,EXTENDER CARD	EMR	205-89-00501	
43	3	016-89-00148	28617	BRKT,ASSY,PWA MOUNTING	EMR	016-89-00148	
45	AR	060-21-00002		CMPD,HEAT CONDUCTIVE GEL	DOW CORNING	DOW CORNING 340	
46	AR	060-11-00002		CMPD,LOCKING,FINE THREAD	LOCTITE CORP	LOCTITE GRADE H	
47	AR	060-11-00010		CMPD,ADHESIVE,FAST SET	EASTMAN	910	

FIRST USAGE MODEL 0720-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
48	1	070-98-00028		CORD,POWER,W/PLUG & RCPT	BELDEN/MML36	17250	
49	1	063-98-00063		CONN,RECP,52PIN,R&P	AMPHENOL	220-2N052	
50	1	047-98-00001		CLAMP,CABLE	AMPHENOL	220-5	
51	52	065-98-00005		CONT, RELIA-TAC, MALE	AMPHENOL	220-P02	
54	AR	276-98-00064		WIRE,#18,STRD,WHT,600V	MML42	NAS-703-18-U-C-9	
55	AR	276-02-00014		WIRE,#22,STRD,TW PR,600V	PRCMT OPTION	MIL-W-16878/4*STL CTD*	
56	AR	276-99-00009	619-24	WIRE,#24,BUSS,SOLID	EMR	276-99-00009	
57	AR	276-98-00081		WIRE,#22,STRD,WHT,600V	MML42	NAS-703-22-U-C-9	
59	AR	229-02-00074		SCREW,4-40X5/16 PAN HD	PRCMT OPTION	MS51957-14	* P
60	1	154-99-00011	20948	LENS,DISPLAY	EMR	154-99-00011	
61	1	154-99-00010	20947	LENS,DISPLAY	EMR	154-99-00010	
62	AR	287-02-00002		NUT,HEX, 4-40	PRCMT OPTION	MS35649-244	
63	AR	229-02-00088		SCREW,6-32X5/8 PAN HD	PRCMT OPTION	MS51957-31	* P
64	AR	229-02-00085		SCREW,6-32X3/8 PAN HD	PRCMT OPTION	MS51957-28	* P
65	AR	229-02-00191		SCREW,4-40X3/4,FLT HD	PRCMT OPTION	MS51959-19	* P
66	AR	229-02-00083		SCREW,6-32X1/4 PAN HD	PRCMT OPTION	MS51957-26	* P
67	AR	229-02-00084		SCREW,6-32X5/16 PAN HD	PRCMT OPTION	MS51957-27	* P
68	AR	273-02-00025		WASHER,#4,INT TOOTH	PRCMT OPTION	MS35333-70	
69	AR	273-02-00026		WASHER,#6,INT TOOTH	PRCMT OPTION	MS35333-71	
70	AR	273-02-00027		WASHER,#8,INT TOOTH	PRCMT OPTION	MS35333-72	
71	AR	273-02-00028		WASHER,#10,INT TOOTH	PRCMT OPTION	MS35333-73	
72	AR	287-02-00003		NUT,HEX, 6-32	PRCMT OPTION	MS35649-264	
73	AR	229-02-00229		SCREW,10-32X1/2 FLAT HD.	QVL	MS24693-C272	* Q
74	4	297-98-00131		STDF,3/8 DIA,10-32X3/4L	AMATOM	8517-SS-1032-0	
75	2	229-02-00288		SCREW,10-32X1 PAN HD	PRCMT OPTION	MS51958-67	* P
76	1	273-98-00041		WASHER,#6,FIBRE .141 ID X	H.H. SMITH	2160	
78	AR	229-02-00104		SCREW,8-32X5/8 PAN HD	PRCMT OPTION	MS51957-46	* P
79	AR	229-02-00195		SCREW,6-32X3/8,FLT HD	PRCMT OPTION	MS51959-28	* P
80	1	284-99-00041	28925	RTNR,PWA	EMR	284-99-00041	
81	1	140-99-00221	21968-64	INSUL,CHASSIS	EMR	140-99-00221	
82	1	016-89-00187	30556-2	BRKT,RACK MT,RS,ASSY,HDL	EMR	016-89-00187	
83	1	016-89-00188	30556-3	BRKT,RACK MT,LS,ASSY,HDL	EMR	016-89-00188	
84	1	196-99-00406	33674	PLATE,WARNING,AC PRESENT	EMR	196-99-00406	
85	2	290-97-00022		BUTTON,SWITCH WHITE	CENTRALAB	B-308-WT	* Q
86	1	290-97-00021		BUTTON,SWITCH BLACK	CENTRALAB	B-308-BL	* Q
87	AR	060-12-00004		CMPD,SEALANT,GENL PURPOSE	G.E.	RTV-102	
88	1	166-98-00106		MARKER,LABEL,5/8X3/8	AVERY/DENN	S-610/43-524	
C 1	1	383-15-22002		CAP., .22MF 20% 600V MET.	CDE	MPY-6P22	
CR 1	1	214-98-00022		RECT,BRDG FW, 30.0A, 100V	MOT	MDA990-2/MDA3501	* Q
DS 1	1	151-02-00001		LAMP,INCAND, 28V 40MA	PRCMT OPTION	MS25237-327	
S 1	1	250-89-00113	32767	SW,PB,LITED,10A@125VAC	EMR	250-89-00113	
T 1	1	262-99-00118	24512	XFMR,PRI 105-132V@47-65HZ	EMR	262-99-00118	
REF 1	1	905-07-00241	23588	SPEC,ENGRG,MODEL 720-02	EMR	905-07-00241	
REF 2	1	905-05-00382	28376	VAR CHART,MODEL 720-02	EMR	905-05-00382	
REF 3	1	905-13-00333	33875	WIRING DIAG	EMR	905-13-00333	
REF 4	1	905-25-00055	24362	I/O CONN LIST MOD 720-02	EMR	905-25-00055	
REF 5	1	197-99-00002	14961-1	PKG SYS,19-INCH DRAWER	EMR	197-99-00002	
REF 6	1	905-28-00002	14962	INSTR,PKG,19-INCH DRAWER	EMR	905-28-00002	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 24023 REV DATE 02/06/75 REV LTR A

LIST TITLE PWA,INTERCONNECT CHGE CONT NO. CODE IDENT SHT 1 OF 1
PART NO. 205-89-01378 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00924	24021	PWB,INTERCONNECT	EMR	204-99-00924	
2	AR	060-11-00020		CMPD,EPOXY,GENL PURPOSE	E&C	ECCOBOND 26	
3	AR	276-98-00064		WIRE,#18,STRD,WHT,600V	MML42	NAS-703-18-U-C-9	
4	AR	252-98-00019		TAPE,GLASS CLOTH,3/8 WIDE	3M	27/BY DESCRIPTION	
J 1 THRU J 3	3	063-98-00234		CONN,36 CONTACTS,SGL ROW	CONTINENTAL	K600-13PCSCGDDD36	
J 4	1	063-98-00233		CONN,72 CONTACTS	CONTINENTAL	K600-11-72Y25A	
J 5	1	063-98-00234		CONN,36 CONTACTS,SGL ROW	CONTINENTAL	K600-13PCSCGDDD36	
J 6	1	063-98-00234		CONN,36 CONTACTS,SGL ROW	CONTINENTAL	K600-13PCSCGDDD36	
J 7	1	063-98-00233		CONN,72 CONTACTS	CONTINENTAL	K600-11-72Y25A	
J 8	1	063-98-00233		CONN,72 CONTACTS	CONTINENTAL	K600-11-72Y25A	
J 9 THRU J 11	3	063-98-00234		CONN,36 CONTACTS,SGL ROW	CONTINENTAL	K600-13PCSCGDDD36	
J 12	1	063-98-00233		CONN,72 CONTACTS	CONTINENTAL	K600-11-72Y25A	
J 13	1	063-98-00234		CONN,36 CONTACTS,SGL ROW	CONTINENTAL	K600-13PCSCGDDD36	
J 14	1	063-98-00233		CONN,72 CONTACTS	CONTINENTAL	K600-11-72Y25A	
R 1 THRU R 4	4	616-02-27069		RES,270 OHM 5% 1/4W	ALLEN BRAD	RC07GF271J	
S 1	1	250-99-00080	24111-3	SW,PB,10 STA,9INTLK,1MOM	EMR	250-99-00080	
S 2	1	250-99-00078	24111-1	SW,PB,3 STA,2INTLK,1MOM	EMR	250-99-00078	
S 3	1	250-99-00078	24111-1	SW,PB,3 STA,2INTLK,1MOM	EMR	250-99-00078	
S 4	1	250-99-00077	24111	SW,PB,4 STA,3INTLK,1MOM	EMR	250-99-00077	
REF 1	1	905-01-00976	24020	SCHEM,PWA,INTERCONNECT	EMR	905-01-00976	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 28276 REV DATE 01/09/78 REV LTR E

LIST TITLE PWA,SUBPANEL CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-01587 ECO 55686 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-01056	28275	PWB,SUBPANEL	EMR	204-99-01056	
2	AR	229-02-00069		SCREW,2-56X1/2 PAN HD	PRCMT OPTION	MS51957-7	* P
3	AR	229-02-00075		SCREW,4-40X3/8 PAN HD	PRCMT OPTION	MS51957-15	* P
4	AR	273-02-00004		WASHER,#4, FLT ST STL	PRCMT OPTION	MS15795-803	
5	AR	287-02-00002		NUT,HEX, 4-40	PRCMT OPTION	MS35649-244	
6	AR	229-02-00085		SCREW,6-32X3/8 PAN HD	PRCMT OPTION	MS51957-28	* P
7	AR	273-02-00006		WASHER,#6, FLT ST STL	PRCMT OPTION	MS15795-805	
8	1	239-99-00099	21714	SPACER,TEST POINT	EMR	239-99-00099	
9	2	287-99-00018	1901	NUT BAR,1 THUMBWHEEL SW	EMR	287-99-00018	
10	4	284-98-00001		RET, SWITCH END PIECE	EECO	E-365G	
11	2	287-99-00019	1902	NUT BAR,6 THUMBWHEEL SW	EMR	287-99-00019	
12	AR	273-02-00024		WASHER,#2,INT TOOTH	PRCMT OPTION	MS35333-69	
13	18	239-98-00090		SPACER, 1/4 OD X 5/16L	AMATOM	9225-N-140-4	
14	6	236-98-00071		SOCKET,IC,DIP,14PIN,SLDR	AUGAT/MML21	514-AG11D	* P
15	AR	273-02-00026		WASHER,#6,INT TOOTH	PRCMT OPTION	MS35333-71	
16	AR	273-02-00003		WASHER,#2, FLT ST STL	PRCMT OPTION	MS15795-802	
17	AR	273-02-00025		WASHER,#4,INT TOOTH	PRCMT OPTION	MS35333-70	
18	AR	229-02-00074		SCREW,4-40X5/16 PAN HD	PRCMT OPTION	MS51957-14	* P
19	1	204-99-00693	18904	PWB,PANEL CONNECTOR	EMR	204-99-00693	
20	AR	276-98-00081		WIRE,#22,STRD,WHT,600V	MML42	NAS-703-22-U-C-9	
21	AR	060-11-00020		CMPD,EPOXY,GENL PURPOSE	E&C	ECCOBOND 26	
22	2	290-97-00019		BUTTON,SWITCH BLACK	CENTRALAB	B-312-BL	* Q
23	AR	060-11-00007		CMPD,ADHESIVE,GENERAL-USE	DOW CORNING	RTV 732	
C 1	1	336-12-33003	601	CAP., 3.3MF 10% 15V	EMR	336-12-33003	
DS 1	1	137-98-00019		IND,LED,RED,.200 OD,.340L	XCITON	XC556-2	* P
DS 2	1	137-98-00021		IND,LED,GRN,.200 OD,.340L	XCITON	XC556G-2	* P
DS 3 THRU DS 18	16	137-98-00019		IND,LED,RED,.200 OD,.340L	XCITON	XC556-2	* P
M 1	1	170-89-00002	21856-1	METER,EDGW,HORIZ,0-30	EMR	170-89-00002	
M 2	1	170-99-00036	21856	METER,EDGW,MODIFIED	EMR	170-99-00036	* Q
R 1 THRU R 41	41	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 42 THRU R 49	8	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 52 THRU R 59	8	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 61	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 62	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
S 1	1	250-99-00088	24112	SW,PB,3 STA,3INTLK	EMR	250-99-00088	
S 2	1	250-98-00208		SW,PB, 1STA,MOM	CENTRALAB	027584	
S 3	1	250-98-00185		SW,THUMBWHL,BCD&CMPLM,MKD	EECO	179798	* Q

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
S 4 THRU S 7	4	250-98-00015		SW,THUMBWHL,BCD&CMPLM	EECO	816-G	* U
S 8	1	250-98-00208		SW,PB, 1STA,MOM	CENTRALAB	027584	
S 9	1	250-89-00090	10876	SW,THUMBWHL,STOPPED 1-4	EMR	250-89-00009	
TP 1 THRU TP 4	4	143-98-00008		JACK,TEST PT,PNL TYPE,WHT	E.F.JOHNSON	105-0251-001	* P
U 1	1	435-98-00010		DSPL,LED 7-SEG RED .3IN	H-P/MML41	5082-7730	* P
U 2	1	046-97-00091		IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32	SN7446AN	
U 3	1	046-97-00091		IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32	SN7446AN	
U 4 THRU U 8	5	435-98-00010		DSPL,LED 7-SEG RED .3IN	H-P/MML41	5082-7730	* P
U 9	1	046-97-00091		IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32	SN7446AN	
U 10	1	046-97-00091		IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32	SN7446AN	
U 11	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 12	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 13	1	046-97-00080		IC,HTTL INV	TI/MML32	SN74H04N	
U 14	1	046-97-00091		IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32	SN7446AN	
U 15	1	046-97-00080		IC,HTTL INV	TI/MML32	SN74H04N	
REF 1	1	905-01-00977	24255	SCHEM,PWA,SUB-PANEL	EMR	905-01-00977	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 33871 REV DATE 05/05/77 REV LTR A

LIST TITLE PANEL,ASSY,REAR CHGE CONT NO. CODE IDENT SHT 1 OF 1
PART NO. 191-89-00747 ECO 54853 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	191-99-00808	33870	PANEL,REAR	EMR	191-99-00808	
3	AR	060-11-00030		CMPD,LOCKING,FINE THREAD	LOCTITE CORP	LOCTITE GRADE C	
4	12	255-98-00012		TERM,LUG,SOLDER,.375ID	BIRNBACH	4	
5	12	022-98-00002		BSHG,NYLON,BNC CONNECTOR	MILTON ROSS	10221-N	
6	12	273-98-00045		WASHER,PHENOLIC .385 ID	SEASTROM	5620-89-62	
7	1	126-98-00002		GRILLE,FAN FINGER GUARD	MML44	476143	
8	AR	229-02-00078		SCREW,4-40X5/8 PAN HD	PRCMT OPTION	MS51957-18	* P
9	AR	273-02-00025		WASHER,#4,INT TOOTH	PRCMT OPTION	MS35333-70	
10	AR	287-02-00002		NUT,HEX, 4-40	PRCMT OPTION	MS35649-244	
11	AR	229-02-00074		SCREW,4-40X5/16 PAN HD	PRCMT OPTION	MS51957-14	* P
12	52	065-98-00002		CONT,RELIA-TAC,FEMALE	AMPHENOL	220-S02	
14	AR	276-02-00014		WIRE,#22,STRD,TW PR,600V	PRCMT OPTION	MIL-W-16878/4*SIL CTD*	
15	AR	276-98-00064		WIRE,#18,STRD,WHT,600V	MML42	NAS-703-18-U-C-9	
B 1	1	999-01-00005	28376	BLOWER, *POA VAR*			
F 1	1	999-01-00001	28376	FUSE*POA VAR*			
J 1	1	063-98-00056		CONN,PLUG,52PIN,R&P	AMPHENOL	220-1N052	
J 5 THRU J 15	11	063-02-00014		CONN,RCPT,BHD,BNC COAX	QVL	UG-1094A/U	
J 20	1	063-02-00014		CONN,RCPT,BHD,BNC COAX	QVL	UG-1094A/U	
J 21	1	200-98-00001		POST,BINDING,5WAY BLK	SUP/HH SMITH	DF30BC/257-103	
J 22	1	200-98-00003		POST,BINDING,5WAY MET	SUP/HH SMITH	GP30NC/1835	
P 1	1	114-98-00089		FLTR,EMI, 6.0A, 50-400HZ	CORCOM/MML63	6EF1	
S 1	1	250-98-00082		SW,TOGGLE,DPDT,6A@125VAC	A HART & H	81027CE	
S 2	1	250-98-00186		SWITCH,SLIDE	SWITCHCRAFT	46256LFR	
XF 1	1	134-98-00006		HLDR,FUSE,3AG,RTANG TERM	MML71	342004-L	
REF 1	1	905-13-00333	33875	WIRING DIAG	EMR	905-13-00333	
REF 2	1	905-05-00382	28376	VAR CHART,MODEL 720-02	EMR	905-05-00382	

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E M R - T E L E M E T R Y

PARTS LIST 21819-2 REV DATE 06/21/74 REV LTR

LIST TITLE HTSK,TRANSISTOR,ASSY CHGE CONT NO. CODE IDENT SHT 1 OF /
PART NO. 298-89-00030 ECO 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	298-89-00031	28375	HTSK,TRANSISTOR,SUBASSY	EMR	298-89-00031	
2	1	298-98-00021		HTSK,THRM RES-7*C/W TO-3	THERMALLOY	6104B	
3	7	022-98-00003		BSHG,SHLDR,NYLON,.115ID	DEL BLINN	NY-04-090	
4	3	140-98-00017		INS,ANDZ ALUMINUM,TO-3	BENDIX	216-6103	* Q
5	3	255-98-00004		TERM,LUG,SOLDER,.120ID	ZIERICK	409	
6	AR	060-11-00002		CMPD,LOCKING,FINE THREAD	LOCTITE CORP	LOCTITE GRADE H	
7	AR	229-02-00077		SCREW,4-40X1/2 PAN HD	PRCMT OPTION	MS51957-17	* P
8	AR	287-02-00002		NUT,HEX, 4-40	PRCMT OPTION	MS35649-244	
9	AR	229-02-00078		SCREW,4-40X5/8 PAN HD	PRCMT OPTION	MS51957-18	* P
10	AR	060-21-00002		CMPD,HEAT CONDUCTIVE GEL	DOW CORNING	DOW CORNING 340	
Q 1	1	263-10-30550		XSTR,NPN 15A SW-AMPL 100V	JEDEC	2N3055	
Q 2	1	263-10-30550		XSTR,NPN 15A SW-AMPL 100V	JEDEC	2N3055	
Q 3	1	263-16-40330		XSTR,NPN,DARLINGTON TO-3	MOT	MJ-4033	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 20457 REV DATE 04/16/76 REV LTR J

LIST TITLE PWA,SOURCE SELECT CHGE CONT NO. CODE IDENT SHT 1 OF 3
PART NO. 205-89-01104 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-89-00416	20456	PWB,SOURCE SELECT	EMR	204-89-00416	
2	AR	276-02-00048		WIRE,#24,SOL, WHT, 600V	PRCMT OPTION	MIL-W-16878/4*SIL CTD*	
3	AR	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN	100-000-NY	
4	AR	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*	EMR	189-99-00005	
5	AR	189-99-00002	800-2	PAD,XSTR TO-5 6 PIN,.075	EMR	189-99-00002	
6	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
7	1	299-99-00001	6477	EJCTR,CARD,.062BD,POSN1	EMR	299-99-00001	
8	2	255-98-00142		TERM.,MICRO-CLIP,PUSH-IN	VECTOR ELECT	T42-1	
C 1	1	304-08-03009	600	CAP. 30PF .5PF 500V	EMR	304-08-03009	
C 2	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 3	1	304-08-02409	600	CAP.,24PF .5PF 500V	EMR	304-08-02409	
C 4	3	304-62-10000	600	CAP. 1000PF 1% 100V	EMR	304-62-10000	
THRU							
C 6							
C 7	1	301-03-10001		CAP,CR , 50V .010 UF 20%	MML 48	8121-05 -651-103M/MML	
C 8	1	301-03-10001		CAP,CR , 50V .010 UF 20%	MML 48	8121-050-651-103M/MML	
C 9	5	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
THRU							
C 13							
C 14	1	320-98-00008		CAP.,TRIMMER,5.5-18PF	MML 23	538-C06,5.5-18PF,A	
C 15	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-05 -651-105M/MML	
C 16	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 17	1	326-21-24004		CAP, 24UF 20% 60V INSUL	SPRAG/TANSIT	111D/TPF*BY DESCR*	* U
C 18	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 19	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 20	1	304-13-06209	600	CAP. 62PF 1% 500V	EMR	304-13-06209	
C 21	1	304-41-62009	600	CAP. 620PF 1% 300V	EMR	304-41-62009	
C 22	1	304-13-06209	600	CAP. 62PF 1% 500V	EMR	304-13-06209	
CR 1	AR	276-99-00008	619-22	WIRE,#22,BUSS,SOLID	EMR	276-99-00008	
CR 2	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 3	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 4	1	088-99-00129	642-05	DIODE,ZENER 0.4W 5.1V	EMR	088-99-00129	
CR 6	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 7	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 8	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 9	1	088-99-00119	642-13	DIODE,ZENER 0.4W 12.0V	EMR	088-99-00119	
CR 10	1	088-99-00329	642-07	DIODE,ZENER 0.4W 6.2V	EMR	088-99-00329	
CR 11	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
Q 1	1	263-10-22221		XSTR,NPN 75V,DC/UHF AMPL	MML 4	2N2222A	
Q 2	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 3	1	263-10-51790		XSTR,NPN VHF CONVERTERS	JEDEC	2N5179	
Q 4	1	263-16-00234		XSTR,NPN,DUAL,DIFF AMPL	MOT	MD1120	
Q 5	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
Q 6	3	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
THRU							
Q 8							

FIRST USAGE MODEL 072

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
Q 9	1	263-92-00089	3902	XSTR,MATCHED SET	EMR	263-92-00089	
Q 10	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
R 1	1	201-98-00015		POT,TRMR 1 K 10% 1W	MML 27	3810P-1-2	* Q
R 2	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 3	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 4	4	616-02-07509		RES. 75 OHM 5% 1/4W	ALLEN BRAD	RC07GF750J	
THRU							
R 7							
R 8	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 9	1	608-09-69800	624	RES, 6.98K 1% 1/10W	EMR	608-09-6980	* P
R 10	1	608-09-14000	624	RES. 1.40K 1% 1/10W	EMR	608-09-14003	* P
R 11	1	608-09-05119	624	RES. 51.1OHM 1% 1/10W	EMR	608-09- 5119	* P
R 12	1	608-09-05119	624	RES. 51.1OHM 1% 1/10W	EMR	608-09- 5119	
R 13	1	608-09-12400	624	RES, 1.24K 1% 1/10W	EMR	608-09-12401	* P
R 14	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 15	1	616-02-75000		RES,7.5K 5% 1/4W	ALLEN BRAD	RC07GF752J	
R 16	1	616-02-16001		RES,16K 5% 1/4W	ALLEN BRAD	RC07GF163J	
R 17	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 19	1	616-02-07509		RES. 75 OHM 5% 1/4W	ALLEN BRAD	RC07GF750J	
R 20	1	616-02-04709		RES,47 OHM 5% 1/4W	ALLEN BRAD	RC07GF470J	
R 21	1	616-02-04709		RES,47 OHM 5% 1/4W	ALLEN BRAD	RC07GF470J	
R 22	1	608-09-00000	20457	RES,*TVAR* 1% 1/10W			
R 23	4	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-5110	* P
THRU							
R 26							
R 27	1	608-09-82509	624	RES. 825 OHM 1% 1/10W	EMR	608-09-82509	* P
R 28	1	608-09-05119	624	RES. 51.1OHM 1% 1/10W	EMR	608-09-5119	* P
R 29	1	608-09-11509	624	RES, 115.0 OHM 1% 1/10W	EMR	608-09-11509	* P
R 30	1	608-09-28001	624	RES, 28.0K 1% 1/10W	EMR	608-09-28001	* P
R 31	1	616-02-75000		RES,7.5K 5% 1/4W	ALLEN BRAD	RC07GF752J	
R 32	1	616-02-16001		RES,16K 5% 1/4W	ALLEN BRAD	RC07GF163J	
R 33	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 34	1	616-02-30009		RES. 300 OHM 5% 1/4W	ALLEN BRAD	RC07GF301J	
R 35	1	616-02-62009		RES,620 OHM 5% 1/4W	ALLEN BRAD	RC07GF621J	
R 36	4	623-02-10009		RES. 100 OHM 5% 1W	ALLEN BRAD	RC32GF101J	
THRU							
R 39							
R 40	1	608-09-51101	624	RES, 51.1K 1% 1/10W	EMR	608-09-51101	* P
R 41	1	616-02-11009		RES,110 OHM 5% 1/4W	ALLEN BRAD	RC07GF111J	
R 42	1	616-02-75009		RES,750 OHM 5% 1/4W	ALLEN BRAD	RC07GF751J	
R 43	1	608-09-13000	624	RES 1.30K 1% 1/10W	EMR	608-09-1300	* P
R 44	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
R 45	1	616-02-56000		RES,5.6K 5% 1/4W	ALLEN BRAD	RC07GF562J	
R 46	1	616-02-33000		RES,3.3K 5% 1/4W	ALLEN BRAD	RC07GF332J	
R 47	1	616-02-62009		RES,620 OHM 5% 1/4W	ALLEN BRAD	RC07GF621J	
R 48	1	616-02-62009		RES,620 OHM 5% 1/4W	ALLEN BRAD	RC07GF621J	
R 49	1	616-02-51000		RES,5.1K 5% 1/4W	ALLEN BRAD	RC07GF512J	
R 50	1	616-02-04709		RES,47 OHM 5% 1/4W	ALLEN BRAD	RC07GF470J	
R 51	1	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 52	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 53	1	616-02-33000		RES,3.3K 5% 1/4W	ALLEN BRAD	RC07GF332J	
R 54	1	616-02-56000		RES,5.6K 5% 1/4W	ALLEN BRAD	RC07GF562J	
R 55	1	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	
R 56	1	616-02-04709		RES,47 OHM 5% 1/4W	ALLEN BRAD	RC07GF470J	
R 57	1	616-02-51000		RES,5.1K 5% 1/4W	ALLEN BRAD	RC07GF512J	
R 58	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 59	1	608-09-51101	624	RES, 51.1K 1% 1/10W	EMR	608-09-51101	* P
R 60	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 61	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 62	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 63	1	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	
RT 1 THRU RT 6	6	101-98-00002		DEV,CUR RGLT RES,DK50 OHM	VACTEC	VTL2C4	
TP 1	1	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* O
TP 2	1	143-98-00051		JACK,TEST PT,PW TYPE,RED	MML 16	430-102	* P
TP 3	1	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* O
TP 4	1	143-98-00051		JACK,TEST PT,PW TYPE,RED	MML 16	430-102	* P
U 1	1	046-97-00093		IC,TTL DCDR/DRVR,BCD-DEC	TI/MML32	SN74145N	* Q
U 3	1	046-34-00004		IC,LIN AMPL,OPNL	MML 40	LM301AH	
U 4 THRU U 6	3	046-97-00138		IC,LIN COMPTR,DIFF HS	TI/MML40	SN72710L	
U 7	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
U 8	1	046-97-00075		IC,TTL OSMV	TI/MML32	SN74121N	
U 9	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
U 10	1	046-97-00075		IC,TTL OSMV	TI/MML32	SN74121N	
REF 1	1	905-01-00779	20455	SCHEMATIC,PWA,SOURCE SEL	EMR	905-01-00779	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720

E M R - T E L E M E T R Y

PARTS LIST 23738 REV DATE 03/10/77 REV LTR F

LIST TITLE PWA,1ST FILTER POLE PAIR CHGE CONT NO. CODE IDENT SHT 1 OF 4
PART NO. 205-89-01362 ECO 54626 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00911	23737	PWB,1ST FILTER POLE PAIR	EMR	204-99-00911	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00002	6477-1	EJCTR,CARD,.062BD,POSN2	EMR	299-99-00002	
4	1	189-99-00001	800-1	PAD,XSTR TO-5,9 OR 11,4 P	EMR	189-99-00001	
5	26	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN	100-000-NY	
6	14	255-98-00142		TERM.,MICRO-CLIP,PUSH-IN	VECTOR ELECT	T42-1	
7	3	189-98-00011		PAD,XSTR,TO-5 8PIN,.375H	MILTON ROSS	10193-DAP	
8	4	273-98-00047		WASHER,FIBRE .016THK	SEASTROM	5600-40-16	
C 1	1	304-13-05109	600	CAP. 51PF 1% 500V	EMR	304-13-05109	
C 2 THRU C 21	20	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 22	1	338-04-47004	601	CAP., 47MF 5% 20V	EMR	338-04-47004	* Q
C 23 THRU C 25	3	339-02-22005	601	CAP. 220MF 5% 10V	EMR	339-02-22005	
C 26	1	337-04-15004	601	CAP. 15.0MF 5% 20V	EMR	337-04-15004	* Q
C 27	1	336-04-15003	601	CAP., 1.5MF 5% 20V	EMR	336-04-15003	* Q
C 28	1	384-05-15102	949	CAP., .151MF 1% 50V	EMR	384-05-15102	
C 29	1	384-05-15001	949	CAP., .015MF 1% 50V	EMR	384-05-15001	
C 30	1	305-20-12000	600	CAP. 1200PF 1% 500V	EMR	305-20-1200	
C 31	1	304-20-24009	600	CAP. 240PF 1% 500V	EMR	304-20-24009	
C 32	1	304-20-51009	600	CAP. 510PF 1% 500V	EMR	304-20-51009	
C 33	1	338-04-33004	601	CAP., 33MF 5% 20V	EMR	338-04-33004	* Q
C 34	1	336-03-33003	601	CAP., 3.3MF 5% 15V	EMR	336-03-33003	* Q
C 35	1	336-05-33002	601	CAP. .33MF 5% 35V	EMR	336-05-33002	* Q
C 36	1	384-05-33001	949	CAP., .033MF 1% 50V	EMR	384-05-33001	
C 37	1	305-20-27000	600	CAP. 2700PF 1% 500V	EMR	305-20-27000	
C 38	1	339-02-18005	601	CAP. 180MF 5% 10V	EMR	339-02-18005	* Q
C 39	1	339-03-15005	601	CAP, 150UF 5% 15V	EMR	339-03-15005	
C 40 THRU C 45	6	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 46 THRU C 48	3	304-01-00309	600	CAP. 3PF .5PF 500V	EMR	304-01-00309	
C 49	1	304-01-01509	600	CAP. 15PF .5PF 500V	EMR	304-01-01509	
C 50	1	304-01-01509	600	CAP. 15PF .5PF 500V	EMR	304-01-01509	
C 51	1	320-98-00021		CAP. TRMR.,15-60PF	MML 23	538-006,15-60PF,F	
C 52	1	320-98-00021		CAP. TRMR.,15-60PF	MML 23	538-006,15-60PF,F	
C 54	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 55	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
CR 1 THRU CR 8	8	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	

FIRST USAGE MODEL 3725-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
CR 9	1	088-99-00109	642-04	DIODE,ZENER 0.4W 4.7V	EMR	088-99-00109	
CR 10	1	088-10-41480		DIODE,SW,75V/50A,4NS/10MA	JEDEC	1N4148	
CR 11	1	088-10-41480		DIODE,SW,75V/50A,4NS/10MA	JEDEC	1N4148	
CR 12	1	088-10-47331		DIODE,ZENER 1.0W 5.1V	MML64	1N4733A	
CR 13	1	088-10-47331		DIODE,ZENER 1.0W 5.1V	MML64	1N4733A	
CR 14 THRU CR 19	6	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
K 1	1	219-99-00031	28531-24	RELAY,1 FORM A,RHOD CONT	EMR	219-99-00031	
L 1	1	055-98-00056		L,RF, 6.80UH,10%,Q50MIN	MML61	1025-40	
L 2	1	055-98-00057		L,RF, 10.00UH,10%,Q55MIN	MML61	1025-44	
L 3	1	055-98-00056		L,RF, 6.80UH,10%,Q50MIN	MML61	1025-40	
L 4	1	055-98-00057		L,RF, 10.00UH,10%,Q55MIN	MML61	1025-44	
Q 1 THRU Q 26	26	263-10-29451		XSTR,PNP LL CHOPPER HFE	JEDEC	2N2945A	
Q 27	1	263-10-22700		XSTR,NPN 60V RF AMPL,CONV	JEDEC	2N2270	
R 1	1	608-09-15009	624	RES., 150 OHM 1% 1/10W	EMR	608-09-15009	* P
R 2	1	608-09-30109	624	RES, 301.0 OHM 1% 1/10W	EMR	608-09-30109	* P
R 3	1	608-09-60409	624	RES, 604.0 OHM 1% 1/10W	EMR	608-09-60409	* P
R 4	1	608-09-1240J	624	RES, 1.24K 1% 1/10W	EMR	608-09-1240	* P
R 5	1	608-09-24300	624	RES, 2.43K 1% 1/10W	EMR	608-09-2430	* P
R 6	1	608-09-49900	624	RES. 4.99K 1% 1/10W	EMR	608-09-49900	* P
R 7	1	608-09-10001	624	RES. 10K 1% 1/10W	EMR	608-09-10001	* P
R 8 THRU R 13	6	616-02-33000		RES,3.3K 5% 1/4W	ALLEN BRAD	RC07GF332J	
R 14	1	608-09-22109	624	RES, 221.0 OHM 1% 1/10W	EMR	608-09-22109	* P
R 15	1	608-09-44209	624	RES, 442.0 OHM 1% 1/10W	EMR	608-09-44209	* P
R 16	1	608-09-88709	624	RES, 887.0 OHM 1% 1/10W	EMR	608-09-88709	* P
R 17	1	608-09-17400	624	RES, 1.74K 1% 1/10W	EMR	608-09-17400	* P
R 18	1	608-09-35700	624	RES, 3.57K 1% 1/10W	EMR	608-09-35709	* P
R 19	1	608-09-71500	624	RES. 7.15K 1% 1/10W	EMR	608-09-71500	* P
R 20	1	608-09-14301	624	RES, 14.3K 1% 1/10W	EMR	608-09-14301	* P
R 21	1	616-02-75000		RES,7.5K 5% 1/4W	ALLEN BRAD	RC07GF752J	
R 22	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 23	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 24	1	616-02-62001		RES,62K 5% 1/4W	ALLEN BRAD	RC07GF623J	
R 25 THRU R 27	3	616-02-12002		RES,120K 5% 1/4W	ALLEN BRAD	RC07GF124J	
R 28	1	616-02-75000		RES,7.5K 5% 1/4W	ALLEN BRAD	RC07GF752J	
R 29	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 30	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 31	1	616-02-62001		RES,62K 5% 1/4W	ALLEN BRAD	RC07GF623J	
R 32 THRU R 34	3	616-02-12002		RES,120K 5% 1/4W	ALLEN BRAD	RC07GF124J	
R 35 THRU R 40	6	616-02-15000		RES,1.5K 5% 1/4W	ALLEN BRAD	RC07GF152J	

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 41	1	616-02-12000		RES,1.2K 5% 1/4W	ALLEN BRAD	RC07GF122J	
R 42	1	616-02-12000		RES,1.2K 5% 1/4W	ALLEN BRAD	RC07GF122J	
R 43	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 44	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 45	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 46	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 47	1	608-01-01249	624	RES, 12.4 OHMS 1% 1/10W 1	EMR	608-01-01249	
R 48	3	608-09-00000	624	RES.*T/VAR*			
THRU							
R 50							
R 51	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 52	1	608-01-01249	624	RES, 12.4 OHMS 1% 1/10W 1	EMR	608-01-01249	
R 53	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 54	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 55	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 56	1	608-01-01249	624	RES, 12.4 OHMS 1% 1/10W 1	EMR	608-01-01249	
R 57	4	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
THRU							
R 60							
R 61	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 62	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 63	1	616-02-24002		RES,240K 5% 1/4W	ALLEN BRAD	RC07GF244J	
R 64	1	616-02-10002		RES,100K 5% 1/4W	ALLEN BRAD	RC07GF104J	
R 65	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 66	1	623-02-39009		RES, 390 OHM 5% 1W	ALLEN BRAD	RC32GF391J	
R 67	4	608-09-88709	624	RES, 887.0 OHM 1% 1/10W	EMR	608-09-88709	* P
THRU							
R 70							
R 71	1	608-09-44209	624	RES, 442.0 OHM 1% 1/10W	EMR	608-09-44209	* P
R 72	1	608-09-44209	624	RES, 442.0 OHM 1% 1/10W	EMR	608-09-44209	
R 73	1	608-09-15000	624	RES, 1.50K 1% 1/10W	EMR	608-09-15000	* P
R 74	1	608-09-75009	624	RES, 750.0 OHM 1% 1/10W	EMR	608-09-75009	* P
R 75	4	608-09-00000	624	RES. *T/VAR*			
THRU							
R 78							
R 79	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
TP 1	1	143-98-00048		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 5	1	143-98-00011		JACK,TEST PT,PW TYPE,GRN	E F JOHNSON	105-0854-001	* P
TP 6	1	143-98-00014		JACK,TEST PT,PW TYPE,BLU	E F JOHNSON	105-0860-001	* P
TP 7	1	143-98-00015		JACK,TEST PT,PW TYPE,VIO	E F JOHNSON	105-0862-001	* P
TP 8	1	143-98-00010		JACK,TEST PT,PW TYPE,BLK	E F JOHNSON	105-0853-001	* P
U 1	4	046-34-00019		IC,LIN AMPL,V FOL,FET-INP	NSC	LH0033CG	* U
THRU							
U 4							
U 5	3	046-34-00020		IC,LIN AMPL,OPNL HS	MML40	LM318H	
THRU							
U 7							

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
REF 1	1	905-01-00962	23736	SCHEM,PWA,1ST FLTR P PR	EMR	905-01-00962	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

PARTS LIST 23745 REV DATE 03/10/77 REV LTR F

LIST TITLE PWA,2ND FILTER POLE PAIR CHGE CONT NO. CODE IDENT SHT 1 OF 4
PART NO. 205-89-01363 ECO 54626 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00912	23744	PWB,2ND FILTER POLE PAIR	EMR	204-99-00912	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00003	6477-2	EJCTR,CARD,.062BD,POSN3	EMR	299-99-00003	
4	1	189-99-00001	800-1	PAD,XSTR TO-5,9 OR 11,4 P	EMR	189-99-00001	
5	20	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN	100-099-NY	
6	2	255-98-00142		TERM.,MICRO-CLIP,PUSH-IN	VECTOR ELECT	T42-1	
7	4	189-98-00011		PAD,XSTR,TO-5 8PIN,.075H	MILTON ROSS	10193-DAP	
8	3	273-98-00047		WASHER,FIBRE .016THK	SEASTROM	5600-40-16	
C 2	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 3	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 4	1	304-01-00000	600	CAP, *TVAR*			
C 5 THRU C 17	13	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 18	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 19 THRU C 21	3	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 22	1	338-04-47004	601	CAP., 47MF 5% 20V	EMR	338-04-47004	* Q
C 23 THRU C 25	3	339-02-22005	601	CAP. 220MF 5% 10V	EMR	339-02-22005	
C 26	1	337-04-15004	601	CAP. 15.0MF 5% 20V	EMR	337-04-15004	* Q
C 27	1	336-04-15003	601	CAP., 1.5MF 5% 20V	EMR	336-04-15003	* Q
C 28	1	384-05-15102	949	CAP., .151MF 1% 50V	EMR	384-05-15102	
C 29	1	384-05-15001	949	CAP., .015MF 1% 50V	EMR	384-05-15001	
C 30	1	305-20-12000	600	CAP. 1200PF 1% 500V	EMR	305-20-12000	
C 31	1	304-20-24009	600	CAP. 240PF 1% 500V	EMR	304-20-24009	
C 32	1	304-20-24009	600	CAP. 240PF 1% 500V	EMR	304-20-24009	
C 33	1	338-14-15004	601	CAP., 15MF 10% 35V	EMR	338-14-15004	
C 34	1	336-13-15003		CAP., 1.5MF 10% 20V	SPEC	601	
C 35	1	384-05-15102	949	CAP., .151MF 1% 50V	EMR	384-05-15102	
C 36	1	384-05-15001	949	CAP., .015MF 1% 50V	EMR	384-05-15001	
C 37	1	305-20-12000	600	CAP. 1200PF 1% 500V	EMR	305-20-12000	
C 38	1	339-03-15005	601	CAP, 150UF 5% 15V	EMR	339-03-15005	
C 39	1	304-01-00309	600	CAP. 3PF .5PF 500V	EMR	304-01- 0309	
C 40 THRU C 45	6	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 46	1	304-01-00309	600	CAP. 3PF .5PF 500V	EMR	304-01-00309	
C 48	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-05 -651-104M/MML	
C 49	1	304-01-00309	600	CAP. 3PF .5PF 500V	EMR	304-01-00309	
CR 1 THRU CR 8	8	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
CR 9	1	088-99-00109	642-04	DIODE,ZENER 0.4W 4.7V	EMR	088-99-00109	
CR 10	6	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
THRU							
CR 15							
K 1	1	219-99-00031	28531-24	RELAY,1 FORM A,RHOD CONT	EMR	219-99-00031	
Q 1	26	263-10-29451		XSTR,PNP LL CHOPPER HFE	JEDEC	2N2945A	
THRU							
Q 26							
Q 27	1	263-10-22700		XSTR,NPN 60V RF AMPL,CONV	JEDEC	2N2270	
R 1	1	608-09-20509	624	RES, 205.0 OHM 1% 1/10W	EMR	608-09-20509	* P
R 2	1	608-09-41209	624	RES, 412.0 OHM 1% 1/10W	EMR	608-09-41209	* P
R 3	1	608-09-82509	624	RES. 825 OHM 1% 1/10W	EMR	608-09-82509	* P
R 4	1	608-09-16500	624	RES. 1.65K OHM 1% 1/10W	EMR	608-09-16500	* P
R 5	1	608-09-32400	624	RES. 3.24K 1% 1/10W	EMR	608-09-32400	* P
R 6	1	608-09-64900	624	RES, 6.49K 1% 1/10W	EMR	608-09-64900	* P
R 7	1	608-09-13001	624	RES, 13.0K 1% 1/10W	EMR	608-09-13001	* P
R 8	6	616-02-33000		RES,3.3K 5% 1/4W	ALLEN BRAD	RC07GF332J	
THRU							
R 13							
R 14	1	608-09-15409	624	RES, 154.0 OHM 1% 1/10W	EMR	608-09-15409	* P
R 15	1	608-09-31609	624	RES, 316.0 OHM 1% 1/10W	EMR	608-09-31609	* P
R 16	1	608-09-63409	624	RES, 634.0 OHM 1% 1/10W	EMR	608-09-63409	* P
R 17	1	608-09-12700	624	RES. 1.27K 1% 1/10W	EMR	608-09-12700	* P
R 18	1	608-09-25500	624	RES, 2.55K 1% 1/10W	EMR	608-09-25500	* P
R 19	1	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-51100	* P
R 20	1	608-09-10201	624	RES, 10.2K 1% 1/10W	EMR	608-09-10201	* P
R 21	1	616-02-75000		RES,7.5K 5% 1/4W	ALLEN BRAD	RC07GF752J	
R 22	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 23	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 24	1	616-02-62001		RES,62K 5% 1/4W	ALLEN BRAD	RC07GF623J	
R 25	3	616-02-12002		RES,120K 5% 1/4W	ALLEN BRAD	RC07GF124J	
THRU							
R 27							
R 28	1	616-02-75000		RES,7.5K 5% 1/4W	ALLEN BRAD	RC07GF752J	
R 29	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 30	1	616-02-30001		RES,30K 5% 1/4W	ALLEN BRAD	RC07GF303J	
R 31	1	616-02-62001		RES,62K 5% 1/4W	ALLEN BRAD	RC07GF623J	
R 32	3	616-02-12002		RES,120K 5% 1/4W	ALLEN BRAD	RC07GF124J	
THRU							
R 34							
R 35	6	616-02-15000		RES,1.5K 5% 1/4W	ALLEN BRAD	RC07GF152J	
THRU							
R 40							
R 41	1	608-09-24900	624	RES, 2.49K 1% 1/10W	EMR	608-09-24900	* P
R 42	1	608-09-20000	624	RES. 2.0K 1% 1/10W	EMR	608-09-20000	* P
R 43	1	608-09-00000	23745	RES. *T VAR*			
R 44	1	608-09-00000	23745	RES. *T VAR*			
R 45	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 46	1	608-09-66509	624	RES, 665.0 OHM 1% 1/10W	EMR	608-09-66509	* P

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 49	1	608-09-00000	624	RES.*T/VAR*			
R 50	1	608-09-00000	624	RES.*T/VAR*			
R 51	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 52	1	608-01-01249	624	RES, 12.4 OHMS 1% 1/10W 1	EMR	608-01-01249	
R 53	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 54	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 55	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 56	1	608-01-01249	624	RES, 12.4 OHMS 1% 1/10W 1	EMR	608-01-01249	
R 57	4	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
THRU							
R 60							
R 61	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 62	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 63	1	616-02-24002		RES,240K 5% 1/4W	ALLEN BRAD	RC07GF244J	
R 64	1	616-02-10002		RES,100K 5% 1/4W	ALLEN BRAD	RC07GF104J	
R 65	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 66	1	623-02-39009		RES, 390 OHM 5% 1W	ALLEN BRAD	RC32GF391J	
R 67	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-1000	* P
R 68	1	608-09-13300	624	RES, 1.33K 1% 1/10W	EMR	608-09-1330	* P
R 69	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-1000	* P
R 70	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-1000	
R 71	1	608-09-24900	624	RES, 2.49K 1% 1/10W	EMR	608-09-2490	* P
R 72	1	608-01-13300	624	RES. 1.33K 1% 1/10W	EMR	608-01-1330	
R 73	1	608-01-10000	624	RES, 1.0K 1% 1/10W	EMR	608-01-1000	
R 74	1	608-01-10000	624	RES, 1.0K 1% 1/10W	EMR	608-01-1000	
R 75	3	608-09-00000	23745	RES. *T VAR*			
THRU							
R 77							
R 78	3	608-01-10000	624	RES, 1.0K 1% 1/10W	EMR	608-01-1000	
THRU							
R 80							
R 81	1	608-09-00000	23745	RES. *T VAR*			
R 82	1	608-09-00000	23745	RES. *T VAR*			
R 83	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-1000	* P
R 84	1	608-09-20000	624	RES. 2.0K 1% 1/10W	EMR	608-09-2000	* P
R 85	1	608-09-00000	624	RES.*T/VAR*			
TP 1	1	143-98-00048		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 5	1	143-98-00011		JACK,TEST PT,PW TYPE,GRN	E F JOHNSON	105-0854-001	* P
TP 6	1	143-98-00014		JACK,TEST PT,PW TYPE,BLU	E F JOHNSON	105-0860-001	* P
TP 7	1	143-98-00015		JACK,TEST PT,PW TYPE,VIO	E F JOHNSON	105-0862-001	* P
TP 8	1	143-98-00016		JACK,TEST PT,PW TYPE,GRA	E F JOHNSON	105-0863-001	* P
TP 9	1	143-98-00023		JACK,TEST PT,PW TYPE,WHT	EF JOHNSON	105-0851-001	* P
TP 10	1	143-98-00010		JACK,TEST PT,PW TYPE,BLK	E F JOHNSON	105-0853-001	* P
U 1	1	046-97-00209		IC,LIN AMPL,OPNL HS SLEW	HARRIS/MML40	HA2-2525-5	
U 2	3	046-34-00019		IC,LIN AMPL,V FOL,FET-INP	NSC	LH0033CG	* U
THRU							
U 4							

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
U 5 THRU U 7	3	046-97-00209		IC,LIN AMPL,OPNL HS SLEW	HARRIS/MML40	HA2-2525-5	
REF 1	1	905-01-00963	23743	SCHEM,PWA,2ND FLTR P PR	EMR	905-01-00963	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

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E M R - T E L E M E T R Y

PARTS LIST 24005 REV DATE 05/14/75 REV LTR B

LIST TITLE PWA, FILTER CONTROL CHGE CONT NO. CODE IDENT SHT 1 OF 3
PART NO. 205-89-01377 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00923	24004	PWB,FILTER CONTROL	EMR	204-99-00923	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	259-99-00004	6477-3	EJCTR,CARD,.0628D,POSN4	EMR	299-99-00004	
4	4	189-98-00016		PAD,XSTR,TO-5 8PIN,.075H	MILTON ROSS	10249-N	
5	4	189-98-00010		PAD,XSTR 10 PIN*USE OPTL*	MILTON ROSS	10247-N	
6	5	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN	100-000-NY	
7	6	255-98-00142		TERM.,MICRO-CLIP,PUSH-IN	VECTOR ELECT	T42-1	
8	1	189-98-00001		PAD,XSTR 3 PIN*USE OPTL*	MILTON ROSS	10028-N	
C 1 THRU C 25	25	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 26 THRU C 33	8	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
C 34	1	304-08-03009	600	CAP. 30PF .5PF 500V	EMR	304-08-03009	
C 35	1	304-01-00309	600	CAP. 3PF .5PF 500V	EMR	304-01-00309	
C 36	1	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
C 37	1	304-01-00000		CAP, *T VAR*			
C 38	1	320-98-00021		CAP. TRMR.,15-60PF	MML 23	538-006,15-60PF,F	
C 39	1	320-98-00021		CAP. TRMR.,15-60PF	MML 23	538-006,15-60PF,F	
C 40	1	320-98-00008		CAP.,TRIMMER,5.5-18PF	MML 23	538-006,5.5-18PF,A	
C 41	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 42 THRU C 44	3	304-01-00309	600	CAP. 3PF .5PF 500V	EMR	304-01-00309	
C 45	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 46	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 47	1	337-04-10004	601	CAP., 10.0MF 5% 20V	EMR	337-04-10004	* Q
C 48	1	337-04-10004	601	CAP., 10.0MF 5% 20V	EMR	337-04-10004	
C 52	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 53	1	301-03-10001		CAP,CR , 50V .010 UF 20%	MML 48	8121-050-651-103M/MML	
C 54	1	301-03-10001		CAP,CR , 50V .010 UF 20%	MML 48	8121-050-651-103M/MML	
CR 1	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 2	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 3	1	088-99-00119	642-13	DIODE,ZENER 0.4W 12.0V	EMR	088-99-00119	
CR 4 THRU CR 17	14	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
L 1	1	055-98-00052		L,RF, 2.20UH,10%,Q30MIN	MML61	1025-28	
L 2	1	055-98-00056		L,RF, 6.80UH,10%,Q50MIN	MML61	1025-40	
L 3	1	055-98-00051		L,RF, 1.00UH,10%,Q25MIN	MML61	1025-20	
L 4	1	055-98-00074		L,RF, 1.50UH,10%,Q28MIN	MML61	1025-24	
L 5	1	055-98-00054		L,RF, 4.70UH,10%,Q45MIN	MML61	1025-36	
L 6	1	055-98-00049		L,RF, 0.68UH,10%,Q28MIN	MML61	1025-16	
Q 1	1	263-10-22700		XSTR,NPN 60V RF AMPL,CONV	JEDEC	2N2270	

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
Q 2	4	263-10-29451		XSTR,PNP LL CHOPPER HFE	JEDEC	2N2945A	
THRU							
Q 5							
Q 6	1	263-10-24321		XSTR,NPN LL CHOPPER 45V	JEDEC	2N2432A	
R 1	8	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
THRU							
R 8							
R 9	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 10	1	616-02-24009		RES. 240 OHM 5% 1/4W	ALLEN BRAD	RC07GF241J	
R 11	4	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
THRU							
R 14							
R 15	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 16	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 17	4	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
THRU							
R 20							
R 21	1	616-02-51001		RES,51K 5% 1/4W	ALLEN BRAD	RC07GF513J	
R 22	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 23	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 24	1	616-02-51001		RES,51K 5% 1/4W	ALLEN BRAD	RC07GF513J	
R 25	3	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
THRU							
R 27							
R 28	1	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-51100	* P
R 29	1	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-51100	
R 30	1	616-02-51001		RES,51K 5% 1/4W	ALLEN BRAD	RC07GF513J	
R 31	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 32	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 33	1	616-02-51001		RES,51K 5% 1/4W	ALLEN BRAD	RC07GF513J	
R 34	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 35	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 36	1	622-02-05609		RES, 56 OHM 5% 1/2W	ALLEN BRAD	RC20GF560J	
R 37	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 38	3	608-09-82509	624	RES. 825 OHM 1% 1/10W	EMR	608-09-82509	* P
THRU							
R 40							
R 41	3	608-09-41209	624	RES, 412.0 OHM 1% 1/10W	EMR	608-09-41209	* P
THRU							
R 43							
R 44	3	608-09-82509	624	RES. 825 OHM 1% 1/10W	EMR	608-09-82509	* P
THRU							
R 46							
R 47	3	616-02-00000	24005	RES *T/VAR*			
THRU							
R 49							
R 50	3	608-09-00000		RES,*TVAR*			
THRU							
R 52							

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 53 THRU R 57	5	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
TP 1	1	143-98-00014		JACK,TEST PT,PW TYPE,BLU	E F JOHNSON	105-0860-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 10	1	143-98-00010		JACK,TEST PT,PW TYPE,BLK	E F JOHNSON	105-0853-001	* P
U 1 THRU U 6	6	046-97-00169		IC,TTL CONV,BCD-TO-BIN	TI/MML32	SN74184N	
U 7	1	046-97-00089		IC,TTL DCDR,BCD-TO-DEC	TI/MML32	SN7442N	
U 8 THRU U 14	7	046-16-00028		IC,LIN AMPL,OPNL	MOT/MML40	MC1437L	
U 15	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 16	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 17	1	046-97-00049		IC,TTL GATE,AND 2-INP	TI/MML32	SN7408N	
U 18	1	046-97-00088		IC,TTL GATE,OR 2-INP	TI/MML32	SN7432N	
U 19	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
U 20	1	046-16-00028		IC,LIN AMPL,OPNL	MOT/MML40	MC1437L	
U 21	1	046-97-00119		IC,HTTL GATE,AND 3-INP	TI/MML32	SN74H11N	
U 22	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML32	SN74S00N	
U 23	1	046-97-00170		IC,STTL GATE,NAND 3-INP	TI/MML32	SN74S10N	
U 24	1	046-97-00170		IC,STTL GATE,NAND 3-INP	TI/MML32	SN74S10N	
U 25	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML32	SN74S00N	
U 26	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML32	SN74S00N	
U 27	1	046-97-00165		IC,STTL INV	TI/MML32	SN74S04N	
U 28	1	046-97-00171		IC,STTL GATE,NAND 4-INP	TI/MML32	SN74S20N	
U 29 THRU U 32	4	046-33-00005		IC,LIN COMPTR,DIFF HS	SIG/NSC	NE529K/LM361H	
U 33 THRU U 35	3	046-34-00020		IC,LIN AMPL,OPNL HS	MML40	LM318H	
U 36	1	046-34-00009		IC,LIN AMPL,OPNL	NSC/MML40	LM2U1AH	
REF 1	1	905-01-00975	24003	SCHEM,PWA FLIR CONTROL	EMR	905-01-00975	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

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PARTS LIST 24019 REV DATE 04/16/76 REV LTR M

LIST TITLE PWA,LOOP FILTER CHGE CONT NO. CODE IDENT SHT 1 OF 6
PART NO. 205-89-01361 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00929	24018	PWB,LOOP FILTER	EMR	204-99-00929	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00005	6477-4	EJCTR,CARD,.062BD,POSN5	EMR	299-99-00005	
4	4	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*	EMR	189-99-00005	
5	6	255-98-00142		TERM.,MICRO-CLIP,PUSH-IN	VECTOR ELECT	T42-1	
6	36	189-99-00003	800-7	PAD,XSTR 4 PIN*USE OPTL*	EMR	189-99-00003	
7	5	189-99-00001	800-1	PAD,XSTR TO-5,9 OR 11,4 P	EMR	189-99-00001	
8	2	273-98-00047		WASHER,FIBRE .016THK	SEASTROM	560C-40-16	
9	1	021-98-00011		BUSBAR,LAM,17 PIN GROUPS	ELDRE CMPNT	ECI-6101-7-17/.3 INCR	* Q
10	AR	276-98-00081		WIRE,#22,STRD,WHT,600V	MML42	NAS-703-22-U-C-9	
11	AR	276-99-00008	619-22	WIRE,#22,BUSS,SOLID	EMR	276-99-00008	
C 1	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR	304-08-02009	
C 2	1	304-20-12009	600	CAP. 120PF 1% 500V	EMR	304-20-12009	
C 3	1	304-20-36009	600	CAP. 360PF 1% 500V	EMR	304-20-36009	
C 4 THRU C 12	9	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 13	1	339-11-22005	601	CAP., 220MF 10% 10V	EMR	339-11-22005	
C 14 THRU C 17	4	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 18	1	305-20-27000	600	CAP. 2700PF 1% 500V	EMR	305-20-27000	
C 19	1	304-20-33009	600	CAP. 330PF 1% 500V	EMR	304-20-33009	
C 20	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 21	1	339-10-33005	601	CAP., 330MF 10% 6V	EMR	339-10-33005	
C 22	1	337-14-33003	601	CAP. 3.3MF 10% 35V	EMR	337-14-33003	
C 23	1	337-02-33004	601	CAP., 33MF 5% 10V	EMR	337-02-33004	* Q
C 24	1	336-14-33002	601	CAP. .33MF 10% 35V	EMR	336-14-33002	
C 25	1	336-05-33001	601	CAP, .033UF 5% 35V	EMR	336-05-33001	* Q
C 26	1	305-20-30000	600	CAP. 3000PF 1% 500V	EMR	305-20-30000	
C 28	1	394-03-10006		CAP., 1000MF 20% 6V	KEMET/MML22	T140D108M006AS	* Q
C 29	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 30	1	305-20-47000	600	CAP. 4700PF 1% 500V	EMR	305-20-47000	
C 31	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 32	1	339-10-33005	601	CAP., 330MF 10% 6V	EMR	339-10-33005	
C 33	1	337-10-47004	601	CAP., 47MF 10% 6V	EMR	337-10-47004	
C 34	1	336-11-47003	601	CAP, 4.7UF 10% 10V	EMR	336-11-47003	* Q
C 35	1	336-05-47002	601	CAP. .47MF 5% 35V	EMR	336-05-47002	* Q
C 36	1	336-08-47001		CAP., .047MF 5% 100V	SPEC	601	* Q
C 39	1	339-12-15005	601	CAP., 150MF 10% 15V	EMR	339-12-15005	
C 40	1	337-04-15004	601	CAP. 15.0MF 5% 20V	EMR	337-04-15004	* Q
C 41	1	336-13-15003		CAP., 1.5MF 10% 20V	SPEC	601	
C 42	1	336-14-15002	601	CAP, .15UF 10% 35V	EMR	336-14-15002	
C 43	1	336-17-15001		CAP., .015MF 10% 100V	SPEC	601	
C 44	1	305-20-15000	600	CAP. 1500PF 1% 500V	EMR	305-20-15000	

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
C 45	1	339-10-33005	601	CAP., 330MF 10% 6V	EMR	339-10-33005	
C 46	1	337-02-33004	601	CAP., 33MF 5% 10V	EMR	337-02-33004	* Q
C 47	1	337-14-33003	601	CAP. 3.3MF 10% 35V	EMR	337-14-33003	
C 48	1	336-14-33002	601	CAP. .33MF 10% 35V	EMR	336-14-33002	
C 49	1	336-05-33001	601	CAP, .033UF 5% 35V	EMR	336-05-33001	* Q
C 50	1	305-20-30000	600	CAP. 3000PF 1% 500V	EMR	305-20-30000	
C 52	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 53	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 54	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 55	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 56	1	303-61-10009	600	CAP., 100PF 2% 100V	EMR	303-61-10009	
C 57	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 58	1	303-61-20009	600	CAP., 200PF 2% 100V	EMR	303-61-20009	
C 59	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 60	1	301-13-22002		CAP,CR , 50V .220 UF 20%	MML 48	8131-050-651-224M/MML	
C 61	1	304-00-00000	24019	CAP,*TVAR*			
C 62	1	304-20-13009	600	CAP. 130PF 1% 500V	EMR	304-20-13009	
C 63	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 64	1	301-13-22002		CAP,CR , 50V .220 UF 20%	MML 48	8131-050-651-224M/MML	
C 65	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 66	1	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
C 67 THRU C 73	7	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 74	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 75	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 76	1	336-12-33003	601	CAP., 3.3MF 10% 15V	EMR	336-12-33003	
C 77	1	304-20-33009	600	CAP. 330PF 1% 500V	EMR	304-20-33009	
C 78	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR	304-08-02009	
CR 1	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 2	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 3	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 4	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 5 THRU CR 13	9	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 14	1	088-10-09381		DIODE,REF,9V/7.5MA,.001 %	JEDEC	1N938/1N938A/1N938B	
CR 15	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 16 THRU CR 23	8	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 24	1	088-99-00379	642-11	DIODE,ZENER 0.4W 9.1V	EMR	088-99-00379	
CR 25	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 26	1	088-99-00119	642-13	DIODE,ZENER 0.4W 12.0V	EMR	088-99-00119	
CR 27 THRU CR 29	3	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
K 1 THRU K 3	3	219-99-00031	28531-24	RELAY,1 FORM A,RHOD CONT	EMR	219-99-00031	

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
Q 1	12	263-10-29451		XSTR,PNP LL CHOPPER HFE	JEDEC	2N2945A	
THRU							
Q 12							
Q 13	1	263-10-22700		XSTR,NPN 60V RF AMPL,CONV	JEDEC	2N2270	
Q 14	20	263-10-29451		XSTR,PNP LL CHOPPER HFE	JEDEC	2N2945A	
THRU							
Q 33							
Q 34	4	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
THRU							
Q 37							
R 1	1	608-09-15001	624	RES, 15.0K 1% 1/10W	EMR	608-09-15001	* P
R 2	1	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-51100	* P
R 3	1	608-09-28709	624	RES, 287.0 OHM 1% 1/10W	EMR	608-09-28709	* P
R 4	1	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-51100	* P
R 5	1	616-02-30009		RES. 300 OHM 5% 1/4W	ALLEN BRAD	RC07GF301J	
R 6	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 7	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 8	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 9	1	608-09-51100	624	RES, 5.11K 1% 1/10W	EMR	608-09-51100	* P
R 10	1	608-09-25501	624	RES, 25.5K 1% 1/10W	EMR	608-09-25501	* P
R 11	1	616-02-30000		RES,3K 5% 1/4W	ALLEN BRAD	RC07GF302J	
R 12	1	608-01-01249	624	RES, 12.4 OHMS 1% 1/10W 1	EMR	608-01-01249	
R 13	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 14	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 16	1	608-09-59009	624	RES, 590.0 OHM 1% 1/10W	EMR	608-09-59009	* P
R 17	1	608-09-20000	624	RES. 2.0K 1% 1/10W	EMR	608-09-20000	* P
R 18	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 19	1	608-09-30109	624	RES, 301.0 OHM 1% 1/10W	EMR	608-09-30109	* P
R 20	1	608-09-23709	624	RES, 237.0 OHM 1% 1/10W	EMR	608-09-23709	* P
R 21	3	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
THRU							
R 23							
R 24	1	608-09-90909	624	RES, 909.0 OHM 1% 1/10W	EMR	608-09-90909	* P
R 25	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 27	1	608-09-30109	624	RES, 301.0 OHM 1% 1/10W	EMR	608-09-30109	* P
R 28	1	608-09-06989	624	RES, 69.8 OHM 1% 1/10W	EMR	608-09-06989	* P
R 29	6	616-02-12001		RES,12K 5% 1/4W	ALLEN BRAD	RC07GF123J	
THRU							
R 34							
R 35	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 36	5	616-02-10002		RES,100K 5% 1/4W	ALLEN BRAD	RC07GF104J	
THRU							
R 40							
R 42	11	616-02-10002		RES,100K 5% 1/4W	ALLEN BRAD	RC07GF104J	
THRU							
R 52							
R 53	3	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
THRU							
R 55							

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 56	1	616-02-82002		RES,820K 5% 1/4W	ALLEN BRAD	RC07GF824J	
R 57	1	616-02-16004		RES,1.6 MEG 5% 1/4W	ALLEN BRAD	RC07GF165J	
R 58	1	616-02-33003		RES,3.3 MEG 5% 1/4W	ALLEN BRAD	RC07GF335J	
R 59	1	616-02-68003		RES,6.8 MEG 5% 1/4W	ALLEN BRAD	RC07GF685J	
R 60	1	608-09-80600	624	RES, 8.06K 1% 1/10W	EMR	608-09-80602	* P
R 61	1	608-09-16201	624	RES, 16.2K 1% 1/10W	EMR	608-09-16201	* P
R 62	1	608-09-32401	624	RES, 32.4K 1% 1/10W	EMR	608-09-32401	* P
R 63	1	608-09-63401	624	RES, 63.4K 1% 1/10W	EMR	608-09-63401	* P
R 64	1	608-09-13302	624	RES, 133.0K 1% 1/10W	EMR	608-09-13302	* P
R 65	1	616-02-13004		RES,13 MEG 5% 1/4W	ALLEN BRAD	RC07GF136J	
R 66	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 67	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 68	1	616-02-24009		RES. 240 OHM 5% 1/4W	ALLEN BRAD	RC07GF241J	
R 69	5	616-02-22009		RES,220 OHM 5% 1/4W	ALLEN BRAD	RC07GF221J	
THRU							
R 73							
R 74	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 75	1	608-09-24309	624	RES, 243.0 OHM 1% 1/10W	EMR	608-09-24309	* P
R 76	1	608-09-24309	624	RES, 243.0 OHM 1% 1/10W	EMR	608-09-24309	
R 77	1	648-53-15700		RES, 1570 OHM .1% .3W	VISHAY	V53-1 OR S102	
R 78	1	608-09-18200	624	RES, 1.82K 1% 1/10W	EMR	608-09-18200	* P
R 79	1	608-09-28709	624	RES, 287.0 OHM 1% 1/10W	EMR	608-09-28709	* P
R 80	1	648-53-15700		RES, 1570 OHM .1% .3W	VISHAY	V53-1 OR S102	
R 81	5	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	
THRU							
R 85							
R 86	1	608-09-37409	624	RES, 374.0 OHM 1% 1/10W	EMR	608-09-37409	* P
R 87	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 88	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 89	1	201-98-00211		POT,TRMR,1.0 K 5% .5W	VISHAY	1202-P-1K	* K
R 90	1	608-09-11509	624	RES, 115.0 OHM 1% 1/10W	EMR	608-09-11509	* P
R 91	1	608-09-28009	624	RES, 280.0 OHM 1% 1/10W	EMR	608-09-28009	* P
R 92	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
R 93	1	608-09-28009	624	RES, 260.0 OHM 1% 1/10W	EMR	608-09-28009	* P
R 94	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
R 95	1	608-09-78709	624	RES, 787.0 OHM 1% 1/10W	EMR	608-09-78709	* P
R 96	1	608-09-17400	624	RES, 1.74K 1% 1/10W	EMR	608-09-17400	* P
R 97	1	608-09-17400	624	RES, 1.74K 1% 1/10W	EMR	608-09-17400	
R 98	1	608-09-78709	624	RES, 787.0 OHM 1% 1/10W	EMR	608-09-78709	* P
R 99	1	648-53-11500		RES, 1150 OHM .1% .3W	VISHAY	V53-1 OR S102	
R 100	1	201-98-00210		POT,TRMR,100 OHM 5% .5W	VISHAY	1202-P-100	* K
R 101	1	648-53-11500		RES, 1150 OHM .1% .3W	VISHAY	V53-1 OR S102	
R 102	1	201-98-00210		POT,TRMR,100 OHM 5% .5W	VISHAY	1202-P-100	* K
R 103	1	648-53-11500		RES, 1150 OHM .1% .3W	VISHAY	V53-1 OR S102	
R 104	1	608-09-04999	624	RES, 49.9 OHM 1% 1/10W	EMR	608-09-04999	* P
R 105	1	608-09-00000	24019	RES,*TVAR*			
R 106	1	201-98-00250		POT,TRMR,500 OHM 5% .5W	VISHAY	1202-P-500	
R 107	1	608-09-39200	624	RES. 3.92K 1% 1/10W	EMR	608-09-39200	* P
R 108	1	608-09-24909	624	RES, 249.0 OHM 1% 1/10W	EMR	608-09-24909	* P

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 109	1	201-98-00250		POT,TRMR,500 OHM 5% .5W	VISHAY	1202-P-500	
R 110	1	608-09-11509	624	RES, 115.0 OHM 1% 1/10W	EMR	608-09-11509	* P
R 111	1	616-02-10009		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 112	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 113	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 114	1	608-09-36501	624	RES. 36.5K 1% 1/10W	EMR	608-09-36501	* P
R 115	1	608-09-46401	624	RES, 46.4K 1% 1/10W	EMR	608-09-46401	* P
R 116	1	616-02-20001		RES,20K 5% 1/4W	ALLEN BRAD	RC07GF203J	
R 117	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 118	1	616-02-75009		RES,750 OHM 5% 1/4W	ALLEN BRAD	RC07GF751J	
R 119	1	616-02-12001		RES,12K 5% 1/4W	ALLEN BRAD	RC07GF123J	
R 120	1	616-02-05609		RES,56 OHM 5% 1/4W	ALLEN BRAD	RC07GF560J	
R 121	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 122	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 123	1	616-02-15001		RES,15K 5% 1/4W	ALLEN BRAD	RC07GF153J	
R 124	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 125	1	608-09-00000	624	RES *T/VAR*			
R 126	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 127	1	608-09-00000	624	RES *T/VAR*			
R 128	1	616-02-00000		RES. *TVAR*			
R 129	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 130	1	608-09-00000		RES,*TVAR*			
RT 1 THRU RT 5	5	101-98-00002		DEV,CUR RGLT RES,DK50 OHM	VACTEC	VTL2C4	
TP 1	1	143-98-00048		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 5	1	143-98-00011		JACK,TEST PT,PW TYPE,GRN	E F JOHNSON	105-0854-001	* P
TP 10	1	143-98-00010		JACK,TEST PT,PW TYPE,BLK	E F JOHNSON	105-0853-001	* P
U 1	1	046-97-00171		IC,STTL GATE,NAND 4-INP	TI/MML32	SN74S20N	
U 2	1	046-97-00170		IC,STTL GATE,NAND 3-INP	TI/MML32	SN74S10N	
U 3	1	046-97-00165		IC,STTL INV	TI/MML32	SN74S04N	
U 4	1	046-97-00171		IC,STTL GATE,NAND 4-INP	TI/MML32	SN74S20N	
U 5	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML32	SN74S00N	
U 6	1	046-15-00003		IC,ARRAY XSTR,3&1DIFF PR	RCA/MML40	CA3045 OR CA3046	
U 7	1	046-15-00003		IC,ARRAY XSTR,3&1DIFF PR	RCA/MML40	CA3045 OR CA3046	
U 8	1	046-34-00017		IC,LIN AMPL,OPNL PRCN	NSC/MML40	LM308AH	
U 9	1	046-34-00021		IC,LIN AMPL,OPNL FET-INP	NSC	LH0062CH	* Q
U 10	1	046-34-00019		IC,LIN AMPL,V FOL,FET-INP	NSC	LH0033CG	* Q
U 11	1	046-34-00019		IC,LIN AMPL,V FOL,FET-INP	NSC	LH0033CG	
U 12	1	046-34-00020		IC,LIN AMPL,OPNL HS	MML40	LM318H	
U 13	1	046-97-00089		IC,TTL DCDR,BCD-TO-DEC	TI/MML32	SN7442N	
U 14	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
U 15	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
U 16 THRU U 20	5	046-97-00190		IC,LIN AMPL,OPNL,COMPEN	MOT/MML40	MC1458P1	

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
U 21	1	046-97-00209		IC,LIN AMPL,OPNL HS SLEW	HARRIS/MML40	HA2-2525-5	
U 22	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
REF 1	1	905-01-00982	24017	SCHEM,PWA,LOOP FILTER	EMR	905-01-00982	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
CR 7	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 8	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 9	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 10	1	088-47-00019		DIODE,SCHOTTKY,15V,20MA	HP/AERTECH	5082-2811/A2S811	
CR 11	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
Q 1	1	263-99-00099	801	XSTR,NPN,SW,HS	EMR	263-99-00099	* Q
Q 2	1	263-99-00099	801	XSTR,NPN,SW,HS	EMR	263-99-00099	
Q 3	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 6	1	263-99-00099	801	XSTR,NPN,SW,HS	EMR	263-99-00099	* Q
Q 9	1	263-99-00099	801	XSTR,NPN,SW,HS	EMR	263-99-00099	* Q
Q 10	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
Q 11	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
Q 12	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 13	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
Q 14	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 15	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 16	1	263-10-22700		XSTR,NPN 60V RF AMPL,CONV	JEDEC	2N2270	
Q 17	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
Q 18	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
R 1	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 2	1	616-02-91009		RES,910 OHM 5% 1/4W	ALLEN BRAD	RC07GF911J	
R 3	1	616-02-24009		RES. 240 OHM 5% 1/4W	ALLEN BRAD	RC07GF241J	
R 4	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 5	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 6	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 7	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 8	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 9	1	608-09-90909	624	RES, 909.0 OHM 1% 1/10W	EMR	608-09-90909	* P
R 10	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 12	1	616-02-18001		RES,18K 5% 1/4W	ALLEN BRAD	RC07GF183J	
R 13	1	616-02-47000		RES,4.7K 5% 1/4W	ALLEN BRAD	RC07GF472J	
R 14	1	608-09-39200	624	RES. 3.92K 1% 1/10W	EMR	608-09-39200	* P
R 15	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 16	1	608-09-49900	624	RES. 4.99K 1% 1/10W	EMR	608-09-49900	* P
R 17	1	608-09-80600	624	RES, 8.06K 1% 1/10W	EMR	608-09-80600	* P
R 18	1	616-02-91009		RES,910 OHM 5% 1/4W	ALLEN BRAD	RC07GF911J	
R 21	1	616-02-91009		RES,910 OHM 5% 1/4W	ALLEN BRAD	RC07GF911J	
R 24	1	608-09-12100	624	RES. 1.21K OHM 1% 1/10W	EMR	608-09-12100	* P
R 25	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 26	1	608-09-12100	624	RES. 1.21K OHM 1% 1/10W	EMR	608-09-12100	* P
R 28	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 29	1	608-09-20000	624	RES. 2.0K 1% 1/10W	EMR	608-09-20000	* P
R 30	1	608-09-20000	624	RES. 2.0K 1% 1/10W	EMR	608-09-20000	
R 31	1	616-02-22000		RES,2.2K 5% 1/4W	ALLEN BRAD	RC07GF222J	
R 32	1	608-09-66500	624	RES, 6.65K 1% 1/10W	EMR	608-09-66500	* P
R 33	1	608-09-11301	624	RES, 11.3K 1% 1/10W	EMR	608-09-11301	* P
R 34	1	616-02-15000		RES,1.5K 5% 1/4W	ALLEN BRAD	RC07GF152J	
R 35	1	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	
R 36	1	608-09-80600	624	RES, 8.06K 1% 1/10W	EMR	608-09-80600	* P

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 37	1	608-09-49900	624	RES. 4.99K 1% 1/10W	EMR	608-09-49900	* P
R 38	1	608-09-00000		RES,*T/VAR*			
R 39	1	608-09-48700	624	RES, 4.87K 1% 1/10W	EMR	608-09-48700	* P
R 40	1	608-09-66500	624	RES, 6.65K 1% 1/10W	EMR	608-09-66500	* P
R 41	1	608-09-18200	624	RES, 1.82K 1% 1/10W	EMR	608-09-18200	* P
R 42	1	608-09-10001	624	RES. 10K 1% 1/10W	EMR	608-09-10001	* P
R 43	1	608-09-52300	624	RES. 5.23K 1% 1/10W	EMR	608-09-52300	* P
R 44	1	608-09-90900	624	RES. 9.09K 1% 1/10W	EMR	608-09-90900	* P
R 45	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 46	1	616-02-47009		RES,470 OHM 5% 1/4W	ALLEN BRAD	RC07GF471J	
R 47	1	608-09-36500	624	RES, 3.65K 1% 1/10W	EMR	608-09-36500	* P
R 48	1	608-09-00000	624	RES,*TVAR*			
R 49	1	608-09-00000	624	RES,*TVAR*			
R 50	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 51	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	
R 52 THRU R 55	4	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 56	1	616-02-15000		RES,1.5K 5% 1/4W	ALLEN BRAD	RC07GF152J	
R 57	1	201-98-00015		POT,TRMR 1 K 10% 1W	MML 27	3810P-102	* Q
R 58	1	201-98-00293		POT,TRMR,200 OHM 10% .75W	MML27	89PR200	* P
R 59	1	608-09-24300	624	RES, 2.43K 1% 1/10W	EMR	608-09-24300	* P
R 60	1	608-09-10001	624	RES. 10K 1% 1/10W	EMR	608-09-10001	* P
R 61	1	608-09-19600	624	RES, 1.96K 1% 1/10W	EMR	608-09-19600	* P
R 62	1	616-02-01009		RES,10 OHM 5% 1/4W	ALLEN BRAD	RC07GF100J	
R 63	1	623-02-12009		RES, 120 OHM 5% 1W	ALLEN BRAD	RC32GF121J	
R 64	1	616-02-18001		RES,18K 5% 1/4W	ALLEN BRAD	RC07GF183J	
R 65	1	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	
R 66	1	616-02-47000		RES,4.7K 5% 1/4W	ALLEN BRAD	RC07GF472J	
R 67	1	616-02-11000		RES,1.1K 5% 1/4W	ALLEN BRAD	RC07GF112J	
R 68	1	616-02-10004		RES,10 MEG 5% 1/4W	ALLEN BRAD	RC07GF106J	
R 69	1	201-98-00040		POT,TRMR 20 K 10% 1W	MML 27	3810P-203	* Q
R 70	1	616-02-10002		RES,100K 5% 1/4W	ALLEN BRAD	RC07GF104J	
R 71	1	616-02-10009		RES,100 OHM 5% 1/4W	ALLEN BRAD	RC07GF101J	
R 72	1	201-98-00292		POT,TRMR,100 OHM 10% .75W	MML27	89PR100	* P
R 73	1	608-09-00000	624	RES. *TVAR*			
R 74	1	616-02-00000	23741	RES,*TVAR*			
R 75	1	616-02-00000	23741	RES,*TVAR*			
R 76	1	608-09-00000	624	RES, *TVAR*			
R 77	1	201-98-00266		POT,TRMR, 1.0 K 10% .5W	BECK/MML27	72PMR1K	* P
TP 1	1	143-98-00008		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 5	1	143-98-00011		JACK,TEST PT,PW TYPE,GRN	E F JOHNSON	105-0854-001	* P
TP 6	1	143-98-00014		JACK,TEST PT,PW TYPE,BLU	E F JOHNSON	105-0860-001	* P
TP 7	1	143-98-00015		JACK,TEST PT,PW TYPE,VIO	E F JOHNSON	105-0862-001	* P
TP 8	1	143-98-00016		JACK,TEST PT,PW TYPE,GRA	E F JOHNSON	105-0863-001	* P
TP 9	1	143-98-00023		JACK,TEST PT,PW TYPE,WHT	EF JOHNSON	105-0851-001	* P

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
U 1	1	046-97-00069		IC,TTL CNTR,DECADE ASYN	TI/MML32	SN7490N	
U 2	1	046-97-00251		IC,TTL CNTR/LCH,DECADE	TI/MML32	SN74196N	
U 3	1	046-97-00251		IC,TTL CNTR/LCH,DECADE	TI/MML32	SN74196N	
U 4	1	046-97-00069		IC,TTL CNTR,DECADE ASYN	TI/MML32	SN7490N	
U 5	1	046-97-00176		IC,STTL MUX, 8-INP	TI/MML32	SN74S151N	
U 6	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
U 7	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 8	1	046-16-00026		INTCKT,PHASE FREQ DET	MOT	MC4044P	
U 9	1	046-97-00069		IC,TTL CNTR,DECADE ASYN	TI/MML32	SN7490N	
U 10	1	046-97-00069		IC,TTL CNTR,DECADE ASYN	TI/MML32	SN7490N	
U 11	1	046-97-00152		IC,STTL FF,D POS EDGE	TI/MML32	SN74S74N	
U 12	1	046-97-00161		IC,HTTL GATE,NAND 4-INP	TI/MML32	SN74H20N	
U 13	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML32	SN74S00N	
U 14	1	046-97-00069		IC,TTL CNTR,DECADE ASYN	TI/MML32	SN7490N	
U 15	1	046-97-00075		IC,TTL OSMV	TI/MML32	SN74121N	
U 16	1	046-16-00028		IC,LIN AMPL,OPNL	MOT/MML40	MC1437L	
U 17	1	046-97-00069		IC,TTL CNTR,DECADE ASYN	TI/MML32	SN7490N	
U 18	1	046-97-00075		IC,TTL OSMV	TI/MML32	SN74121N	
U 19	1	046-11-00037		IC,HTTL FF,J-K TYPE	TI	SN74H103N	* Q
U 20 THRU U 23	4	046-97-00110		IC,TTL CNTR,DECADE UP/DN	TI/MML32	SN74190N	* K
U 24	1	046-97-00068		IC,TTL GATE,EXCL-OR 2-INP	TI/MML32	SN7486N	
U 25	1	046-11-00037		IC,HTTL FF,J-K TYPE	TI	SN74H103N	* Q
U 26	1	046-97-00103		IC,TTL MUX, 8-INP	TI/MML32	SN74151N	
U 27	1	046-34-00009		IC,LIN AMPL,OPNL	NSC/MML40	LM201AH	
REF 1	1	905-01-00961	23739	SCHEMATIC,PWA,VCO	EMR	905-01-00961	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

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E M R - T E L E M E T R Y

PARTS LIST 20481 REV DATE 07/21/77 REV LTR G

LIST TITLE PWA,BIT RATE STORE CHGE CONT NO. CODE IDENT SHT 1 OF 1
PART NO. 205-89-01110 ECO 55191 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00734	20480	PWB,BIT RATE STORE	EMR	204-99-00734	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00007	6477-6	EJCTR,CARD,.062BD,POSN7	EMR	299-99-00007	
4	AR	276-98-00081		WIRE,#22,STRD,WHT,600V	MML42	NAS-703-22-U-C-9	
C 1	1	304-62-10000	600	CAP. 1000PF 1% 100V	EMR	304-62-10000	
C 2	1	336-14-10003	601	CAP. 1.0MF 10% 35V	EMR	336-14-10003	
C 3	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
R 1	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 2	1	616-02-18009		RES,180 OHM 5% 1/4W	ALLEN BRAD	RC07GF181J	
R 3	1	622-02-10009		RES. 100 OHM 5% 1/2W	ALLEN BRAD	RC20GF101J	
R 4 THRU R 20	17	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
TP 1	1	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* Q
TP 2 THRU TP 4	3	143-98-00051		JACK,TEST PT,PW TYPE,RED	MML 16	430-102	* P
U 1 THRU U 4	4	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	* Q
U 5	1	046-97-00049		IC,TTL GATE,AND 2-INP	TI/MML32	SN7408N	
U 6	1	046-97-00089		IC,TTL DCDR,BCD-TO-DEC	TI/MML32	SN7442N	
U 7 THRU U 10	4	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 11	1	046-97-00094		IC,TTL DCDR,BCD-TO-1OF16	TI/MML32	SN74154N	
U 12	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
REF 1	1	905-01-00786	20479	SCHEMATIC,PWA,BIT RATE ST	EMR	905-01-00786	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-01

E M R - T E L E M E T R Y

PARTS LIST 23996 REV DATE 07/21/77 REV LTR D

LIST TITLE PWA,FORMAT STORE CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. 205-89-01373 ECO 55191 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00920	23995	PWB,FORMAT STORE	EMR	204-99-00920	
2	1	299-98-00002		EJECT., CARD	SCANDE	S-200	
3	1	299-99-00008	6477-7	EJCTR,CARD,.062BD,POSN8	EMR	299-99-00008	
4	AR	276-02-00048		WIRE,#24,SOL, WHT, 600V	PRCMT OPTION	MIL-W-16878/4*SIL CTD*	
C 1	1	336-14-10003	601	CAP. 1.0MF 10% 35V	EMR	336-14-10003	
C 2	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
R 1	25	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
THRU							
R 20							
R 21	1	616-02-20000		RES,2K 5% 1/4W	ALLEN BRAD	RC07GF202J	
R 22	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 23	1	616-02-20000		RES,2K 5% 1/4W	ALLEN BRAD	RC07GF202J	
R 24	3	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
THRU							
R 26							
TP 1	1	143-98-00048		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
U 1	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	* Q
U 2	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	
U 3	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
U 4	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	* Q
U 5	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	
U 6	1	046-97-00049		IC,TTL GATE,AND 2-INP	TI/MML32	SN7408N	
U 7	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	* Q
U 8	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
U 9	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 10	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 11	1	046-97-00050		IC,TTL GATE,NAND 3-INP	TI/MML32	SN7410N	
U 12	1	046-97-00050		IC,TTL GATE,NAND 3-INP	TI/MML32	SN7410N	
U 13	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 14	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 15	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	* Q
U 16	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	
U 17	1	046-97-00049		IC,TTL GATE,AND 2-INP	TI/MML32	SN7408N	
U 18	1	046-97-00105		IC,TTL MUX, 2-INP	TI/MML32	SN74157N	
U 19	1	046-97-00101		IC,LTTL MUX/RGTR,4-BIT	TI/MML32	SN74L98N	* Q
U 25	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
REF 1	1	905-01-00970	23994	SCHEM,PWA,FORMAT STORE	EMR	905-01-00970	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 23876 REV DATE 09/11/75 REV LTR D

LIST TITLE PWA, DC RESTORER CHGE CONT NO. CODE IDENT SHT 1 OF 5
PART NO. 205-89-01366 ECO 52416 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00914	23875	PWB, DC RESTORER	EMR	204-99-00914	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00009	6477-8	EJCTR,CARD,.062BD,PCSN9	EMR	299-99-00009	
4	4	189-98-00016		PAD,XSTR,TO-5 8PIN,.075H	MILTON ROSS	10249-N	
5	1	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN	100-000-NY	
6	5	189-98-00010		PAD,XSTR 10 PIN*USE OPTL*	MILTON ROSS	10247-N	
C 1	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 2	4	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
THRU							
C 5							
C 6	1	337-04-10004	601	CAP., 10.0MF 5% 20V	EMR	337-04-10004	* Q
C 7	1	304-00-00000	600	CAP,' *TVAR*			
C 8	1	304-20-10009	600	CAP. 100PF 1% 500V	EMR	304-20-10009	
C 9	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 10	1	337-05-68003	601	CAP., 6.8MF 5% 35V	EMR	337-05-68003	* Q
C 11	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 12	1	337-05-68003	601	CAP., 6.8MF 5% 35V	EMR	337-05-68003	* Q
C 13	1	304-20-27009	600	CAP. 270PF 1% 500V	EMR	304-20-27009	
C 14	1	304-20-10009	600	CAP. 100PF 1% 500V	EMR	304-20-10009	
C 15	1	304-20-10009	600	CAP. 100PF 1% 500V	EMR	304-20-10009	
C 16	4	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
THRU							
C 19							
C 20	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 21	1	304-20-27009	600	CAP. 270PF 1% 500V	EMR	304-20-27009	
C 22	1	304-20-10009	600	CAP. 100PF 1% 500V	EMR	304-20-10009	
C 23	3	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
THRU							
C 25							
C 26	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
C 27	1	305-20-15000	600	CAP. 1500PF 1% 500V	EMR	305-20-15000	
C 28	1	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
C 29	1	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
C 30	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR	304-08-02009	
C 31	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR	304-08-02009	
C 32	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 33	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 34	1	304-08-03009	600	CAP. 30PF .5PF 500V	EMR	304-08-03009	
C 35	1	305-20-15000	600	CAP. 1500PF 1% 500V	EMR	305-20-15000	
C 36	3	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
THRU							
C 38							
C 39	1	305-20-15000	600	CAP. 1500PF 1% 500V	EMR	305-20-1500	
C 40	1	304-01-01009	600	CAP. 10PF .5PF 500V	EMR	304-01-01009	
C 41	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR	304-08-02009	

FIRST USAGE MODEL 0720-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
C 42	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR	304-08-02009	
C 43	15	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-05[illegible]-651-104M/MML	
THRU							
C 57							
CR 1	8	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
THRU							
CR 8							
CR 9	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 10	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
CR 11	8	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
THRU							
CR 18							
CR 19	4	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
THRU							
CR 22							
CR 23	9	088-99-00199	642-06	DIODE,ZENER 0.4W 5.6V	EMR	088-99-00199	
THRU							
CR 31							
CR 32	1	088-99-00099	642-00	DIODE,ZENER 0.4W 3.3V	EMR	088-99-00099	
Q 1	1	263-10-29451		XSTR,PNP LL CHOPPER HFE	JEDEC	2N2945A	
R 1	1	616-02-68009		RES,680 OHM 5% 1/4W	ALLEN BRAD	RC07GF681J	
R 2	5	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
THRU							
R 6							
R 7	4	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
THRU							
R 10							
R 11	1	616-02-33000		RES,3.3K 5% 1/4W	ALLEN BRAD	RC07GF332J	
R 12	1	608-09-32409	624	RES, 324.0 OHM 1% 1/10W	EMR	608-09-32409	* P
R 13	1	608-09-59000	624	RES, 5.90K 1% 1/10W	EMR	608-09-5900[illegible]	* P
R 14	1	608-09-18700	624	RES, 1.87K 1% 1/10W	EMR	608-09-1870[illegible]	* P
R 15	1	608-09-78709	624	RES, 787.0 OHM 1% 1/10W	EMR	608-09-78709	* P
R 16	1	608-09-60400	624	RES, 6.04K 1% 1/10W	EMR	608-09-6040[illegible]	* P
R 17	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 18	1	608-09-61900	624	RES. 6.19K 1% 1/10W	EMR	608-09-6190[illegible]	* P
R 19	1	608-09-20002	624	RES, 200.0K 1% 1/10W	EMR	608-09-20002	* P
R 20	1	608-09-10002	624	RES, 100.0K 1% 1/10W	EMR	608-09-10002	* P
R 21	1	608-09-49901	624	RES, 49.9K 1% 1/10W	EMR	608-09-49901	* P
R 22	1	608-09-24901	624	RES, 24.9K 1% 1/10W	EMR	608-09-24901	* P
R 23	1	608-09-12401	624	RES, 12.4K 1% 1/10W	EMR	608-09-12401	* P
R 24	1	608-09-00000	624	RES, *TVAR*			
R 25	3	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
THRU							
R 27							
R 28	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
R 29	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-1000[illegible]	* P
R 30	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 31	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 32	4	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
THRU							
R 35							

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 36	1	608-09-32409	624	RES, 324.0 OHM 1% 1/10W	EMR	608-09-32409	* P
R 37	1	608-09-59000	624	RES, 5.90K 1% 1/10W	EMR	608-09-59000	* P
R 38	1	608-09-18700	624	RES, 1.87K 1% 1/10W	EMR	608-09-18700	* P
R 39	1	608-09-78709	624	RES, 787.0 OHM 1% 1/10W	EMR	608-09-78709	* P
R 40	1	608-09-60400	624	RES, 6.04K 1% 1/10W	EMR	608-09-60400	* P
R 41	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 42	1	608-09-61900	624	RES. 6.19K 1% 1/10W	EMR	608-09-61900	* P
R 43	1	608-09-20002	624	RES, 200.0K 1% 1/10W	EMR	608-09-20002	* P
R 44	1	608-09-10002	624	RES, 100.0K 1% 1/10W	EMR	608-09-10002	* P
R 45	1	608-09-49901	624	RES, 49.9K 1% 1/10W	EMR	608-09-49901	* P
R 46	1	608-09-24901	624	RES, 24.9K 1% 1/10W	EMR	608-09-24901	* P
R 47	1	608-09-12401	624	RES, 12.4K 1% 1/10W	EMR	608-09-12401	* P
R 48	1	608-09-00000	624	RES, *TVAR*			
R 49	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	* P
R 50	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR	608-09-10000	
R 51	1	608-09-10009	624	RES, 100.0 OHM 1% 1/10W	EMR	608-09-10009	* P
R 52	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
R 53	1	616-02-51001		RES,51K 5% 1/4W	ALLEN BRAD	RC07GF513J	
R 55	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 56	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 57	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 58	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 59	1	616-02-16001		RES,16K 5% 1/4W	ALLEN BRAD	RC07GF163J	
R 61	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 62	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 63	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 64	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 65	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 66	1	616-02-10002		RES,100K 5% 1/4W	ALLEN BRAD	RC07GF104J	
R 68	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 69	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 70	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 71	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 72	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 73	1	616-02-10001		RES,10K 5% 1/4W	ALLEN BRAD	RC07GF103J	
R 74	1	608-09-10009	624	RES, 100.0 OHM 1% 1/10W	EMR	608-09-10009	* P
R 75	1	616-02-51001		RES,51K 5% 1/4W	ALLEN BRAD	RC07GF513J	
R 77	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 78	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 79	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 80	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 81	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W	EMR	608-09-51109	* P
R 82	1	616-02-16001		RES,16K 5% 1/4W	ALLEN BRAD	RC07GF163J	
R 84	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 85	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 86	1	616-02-20009		RES,200 OHM 5% 1/4W	ALLEN BRAD	RC07GF201J	
R 87	1	616-02-24000		RES,2.4K 5% 1/4W	ALLEN BRAD	RC07GF242J	
R 88	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 89	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
TP 1	1	143-98-00048		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 2	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 3	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 5	1	143-98-00011		JACK,TEST PT,PW TYPE,GRN	E F JOHNSON	105-0854-001	* P
TP 6	1	143-98-00014		JACK,TEST PT,PW TYPE,BLU	E F JOHNSON	105-0860-001	* P
TP 7	1	143-98-00015		JACK,TEST PT,PW TYPE,VIO	E F JOHNSON	105-0862-001	* P
TP 8	1	143-98-00016		JACK,TEST PT,PW TYPE,GRA	E F JOHNSON	105-0863-001	* P
TP 9	1	143-98-00023		JACK,TEST PT,PW TYPE,WHT	EF JOHNSON	105-0851-001	* P
TP 10	1	143-98-00010		JACK,TEST PT,PW TYPE,BLK	E F JOHNSON	105-0853-001	* P
TP 11	1	143-98-00048		JACK,TEST PT,PW TYPE,BRN	E F JOHNSON	105-0858-001	* P
TP 12	1	143-98-00009		JACK,TEST PT,PW TYPE,RED	E F JOHNSON	105-0852-001	* P
TP 13	1	143-98-00012		JACK,TEST PT,PW TYPE,ORN	E F JOHNSON	105-0856-001	* P
TP 14	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
U 1	1	046-97-00152		IC,STTL FF,D POS EDGE	TI/MML32	SN74S74N	
U 2	1	046-97-00152		IC,STTL FF,D POS EDGE	TI/MML32	SN74S74N	
U 3	1	046-97-00048		IC,TTL INV,OPEN-COLL 5.5V	TI/MML32	SN7405N	
U 4	1	046-97-00075		IC,TTL OSMV	TI/MML32	SN74121N	
U 5	1	046-97-00075		IC,TTL OSMV	TI/MML32	SN74121N	
U 6	1	046-97-00071		IC,TTL CNTR,BIN 4-BIT	TI/MML32	SN7493N	
U 7	1	046-97-00071		IC,TTL CNTR,BIN 4-BIT	TI/MML32	SN7493N	
U 8	1	046-97-00170		IC,STTL GATE,NAND 3-INP	TI/MML32	SN74S10N	
U 9	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 10	1	046-97-00044		IC,TTL GATE,NAND 2-INP	TI/MML32	SN7400N	
U 11	1	046-97-00111		IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32	SN74191N	* K
U 12	1	046-97-00111		IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32	SN74191N	
U 13	1	046-97-00048		IC,TTL INV,OPEN-COLL 5.5V	TI/MML32	SN7405N	
U 14	1	046-97-00048		IC,TTL INV,OPEN-COLL 5.5V	TI/MML32	SN7405N	
U 15	1	046-97-00052		IC,TTL GATE,NAND 4-INP	TI/MML32	SN7420N	
U 16	1	046-97-00054		IC,TTL GATE,NAND 8-INP	TI/MML32	SN7430N	
U 17	1	046-97-00048		IC,TTL INV,OPEN-COLL 5.5V	TI/MML32	SN7405N	
U 18	1	046-15-00003		IC,ARRAY XSTR,3&1DIFF PR	RCA/MML40	CA3045 OR CA3046	
U 19	1	046-34-00020		IC,LIN AMPL,OPNL HS	MML40	LM318H	
U 20	1	046-34-00020		IC,LIN AMPL,OPNL HS	MML40	LM318H	
U 21	1	046-97-00111		IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32	SN74191N	* K
U 22	1	046-97-00111		IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32	SN74191N	
U 23	1	046-97-00048		IC,TTL INV,OPEN-COLL 5.5V	TI/MML32	SN7405N	
U 24	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
U 25	1	046-97-00054		IC,TTL GATE,NAND 8-INP	TI/MML32	SN7430N	
U 26	1	046-97-00052		IC,TTL GATE,NAND 4-INP	TI/MML32	SN7420N	
U 27	1	046-97-00050		IC,TTL GATE,NAND 3-INP	TI/MML32	SN7410N	
U 28	1	046-97-00048		IC,TTL INV,OPEN-COLL 5.5V	TI/MML32	SN7405N	
U 29	1	046-15-00003		IC,ARRAY XSTR,3&1DIFF PR	RCA/MML40	CA3045 OR CA3046	
U 30	1	046-34-00020		IC,LIN AMPL,OPNL HS	MML40	LM318H	
U 31	1	046-34-00004		IC,LIN AMPL,OPNL	MML 40	LM301AH	
U 32 THRU U 36	5	046-33-00035		IC,LIN COMPTR,DIFF HS	SIG/NSC	NE529K/LM361H	
U 37	1	046-97-00049		IC,TTL GATE,AND 2-INP	TI/MML32	SN7408N	

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
U 38	1	046-97-00050		IC,TTL GATE,NAND 3-INP	TI/MML32	SN7410N	
U 39	1	046-97-00047		IC,TTL INV	TI/MML32	SN7404N	
REF 1	1	905-01-00965	23874	SCHEMATIC,PWA,DC RESTORER	EMR	905-01-00965	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

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E M R - T E L E M E T R Y

PARTS LIST 23879 REV DATE 04/12/76 REV LTR E

LIST TITLE PWA,CODE CONVERTER CHGE CONT NO. CODE IDENT SHT 1 OF 3
PART NO. 205-89-01376 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00922	23878	PWB,CODE CONVERTER	EMR	204-99-00922	
2	1	259-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00010	6477-9	EJCTR,CARD,.062BD,POSN10	EMR	299-99-00010	
4	1	021-98-00011		BUSBAR,LAM,17 PIN GROUPS	ELDRE CMPNT	ECI-6101-7-17/.3 INCR	* Q
5	3	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*	EMR	189-99-00005	
6	AR	276-99-00008	619-22	WIRE,#22,BUSS,SOLID	EMR	276-99-00008	
7	AR	252-98-00019		TAPE,GLASS CLOTH,3/8 WIDE	3M	27/BY DESCRIPTION	
C 1	1	301-03-47001		CAP,CR , 50V .047 UF 20%	MML 48	8121-050-651-473M/MML	
C 2	1	301-03-10001		CAP,CR , 50V .010 UF 20%	MML 48	8121-050-651-103M/MML	
C 3	4	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
THRU							
C 6							
C 7	1	301-03-47001		CAP,CR , 50V .047 UF 20%	MML 48	8121-050-651-473M/MML	
C 8	1	304-00-00000		CAP,*T/VAR*			
C 9	1	304-13-07509	600	CAP. 75PF 1% 500V	EMR	304-13-07509	
C 10	1	301-03-10001		CAP,CR , 50V .010 UF 20%	MML 48	8121-050-651-103M/MML	
C 11	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 12	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 13	1	339-12-15005	601	CAP., 150MF 10% 15V	EMR	339-12-15005	
C 14	1	304-13-07509	600	CAP. 75PF 1% 500V	EMR	304-13-07509	
C 15	1	337-04-15004	601	CAP. 15.0MF 5% 20V	EMR	337-04-15004	* Q
C 16	1	304-20-00000	600	CAP., *T VAR*			
C 17	1	304-20-12009	600	CAP. 120PF 1% 500V	EMR	304-20-12009	
C 18	1	304-20-12009	600	CAP. 120PF 1% 500V	EMR	304-20-12009	
C 19	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 20	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 21	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 22	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 23	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 24	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR	337-13-10004	
C 25	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 26	1	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
CR 1	1	088-99-00329	642-07	DIODE,ZENER 0.4W 6.2V	EMR	088-99-00329	
CR 2	1	088-99-00329	642-07	DIODE,ZENER 0.4W 6.2V	EMR	088-99-00329	
CR 3	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 4	1	088-99-00329	642-07	DIODE,ZENER 0.4W 6.2V	EMR	088-99-00329	
CR 5	1	088-99-00329	642-07	DIODE,ZENER 0.4W 6.2V	EMR	088-99-00329	
CR 6	3	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
THRU							
CR 8							
R 1	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 2	1	616-02-68000		RES,6.8K 5% 1/4W	ALLEN BRAD	RC07GF682J	
R 3	1	616-02-15002		RES,150K 5% 1/4W	ALLEN BRAD	RC07GF154J	
R 4	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 5	1	608-09-90909	624	RES, 909.0 OHM 1% 1/10W	EMR	608-09-90909	* P

FIRST USAGE MODEL 0720-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 6	1	608-09-16501	624	RES, 16.5K 1% 1/10W	EMR	608-09-16501	* P
R 7	1	608-09-90909	624	RES, 909.0 OHM 1% 1/10W	EMR	608-09-90909	* P
R 8	1	608-09-16501	624	RES, 16.5K 1% 1/10W	EMR	608-09-16501	* P
R 9	1	616-02-68000		RES,6.8K 5% 1/4W	ALLEN BRAD	RC07GF682J	
R 10	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 11	1	616-02-15002		RES,150K 5% 1/4W	ALLEN BRAD	RC07GF154J	
R 12	1	616-02-51009		RES,510 OHM 5% 1/4W	ALLEN BRAD	RC07GF511J	
R 13	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 14	1	616-02-08209		RES,82 OHM 5% 1/4W	ALLEN BRAD	RC07GF820J	
R 15	1	616-02-18009		RES,180 OHM 5% 1/4W	ALLEN BRAD	RC07GF181J	
R 16	1	201-98-00089		POT,TRMR 2 K 10% 1W	MML 27	3810P-202	* Q
R 17	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 18	1	616-02-10000		RES,1K 5% 1/4W	ALLEN BRAD	RC07GF102J	
R 19	1	616-02-15002		RES,150K 5% 1/4W	ALLEN BRAD	RC07GF154J	
R 20	1	616-02-47009		RES,470 OHM 5% 1/4W	ALLEN BRAD	RC07GF471J	
R 21	1	616-02-18009		RES,180 OHM 5% 1/4W	ALLEN BRAD	RC07GF181J	
R 22	1	616-02-33001		RES,33K 5% 1/4W	ALLEN BRAD	RC07GF333J	
R 23	1	616-02-08209		RES,82 OHM 5% 1/4W	ALLEN BRAD	RC07GF820J	
R 24 THRU R 26	3	616-02-47009		RES,470 OHM 5% 1/4W	ALLEN BRAD	RC07GF471J	
R 27	1	616-02-18009		RES,180 OHM 5% 1/4W	ALLEN BRAD	RC07GF181J	
R 28	1	616-02-18009		RES,180 OHM 5% 1/4W	ALLEN BRAD	RC07GF181J	
R 29	1	616-02-47009		RES,470 OHM 5% 1/4W	ALLEN BRAD	RC07GF471J	
S 1	1	250-98-00199		SW,TOGGLE,SPDT,PWB MOUNT	C & K COMP	7101A	* Q
TP 1 THRU TP 13	13	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* Q
U 1	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML 32	SN74S00N	
U 2	1	046-97-00164		IC,STTL GATE,AND 3-INP	TI/MML 32	SN74S11N	
U 3	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML 32	SN74S00N	
U 4	1	046-97-00119		IC,HTTL GATE,AND 3-INP	TI/MML 32	SN74H11N	
U 5	1	046-97-00138		IC,LIN COMPTR,DIFF HS	TI/MML 40	SN72710L	
U 6	1	046-97-00075		IC,TTL OSMV	TI/MML 32	SN74121N	
U 7	1	046-97-00165		IC,STTL INV	TI/MML 32	SN74S04N	
U 8	1	046-97-00081		IC,HTTL GATE,AND-OR-INV	TI/MML 32	SN74H51N	
U 9	1	046-97-00081		IC,HTTL GATE,AND-OR-INV	TI/MML 32	SN74H51N	
U 10	1	046-97-00080		IC,HTTL INV	TI/MML 32	SN74H04N	
U 11	1	046-97-00162		IC,STTL GATE,NAND 2-INP	TI/MML 32	SN74S00N	
U 12	1	046-97-00119		IC,HTTL GATE,AND 3-INP	TI/MML 32	SN74H11N	
U 13	1	046-97-00115		IC,HTTL GATE,NAND 3-INP	TI/MML 32	SN74H10N	
U 14	1	046-97-00166		IC,HTTL GATE,NAND 8-INP	TI/MML 32	SN74H30N	
U 15	1	046-97-00166		IC,HTTL GATE,NAND 8-INP	TI/MML 32	SN74H30N	
U 16	1	046-97-00080		IC,HTTL INV	TI/MML 32	SN74H04N	
U 17	1	046-97-00080		IC,HTTL INV	TI/MML 32	SN74H04N	
U 18	1	046-97-00146		IC,TTL SR,8BIT SER-PRL	TI/MML 32	SN74164N	
U 19	1	046-97-00076		IC,TTL CNTR,DECADE UP/DN	TI/MML 32	SN74192N	
U 20	1	046-11-00036		IC,HTTL FF,D TYPE PCS	TI/MML 32	SN74H74N	
U 21	1	046-97-00167		IC,STTL FF,J-K TYPE W/CLR	TI/MML 32	SN74S112N	

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ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
U 22	1	046-11-00036		IC,HTTL FF,D TYPE POS	TI/MML32	SN74H74N	
U 23	1	046-97-00068		IC,TTL GATE,EXCL-OR 2-INP	TI/MML32	SN7486N	
U 24	1	046-97-00068		IC,TTL GATE,EXCL-OR 2-INP	TI/MML32	SN7486N	
U 25	1	046-97-00152		IC,STTL FF,D POS EDGE	TI/MML32	SN74S74N	
U 26	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 27	1	046-97-00115		IC,HTTL GATE,NAND 3-INP	TI/MML32	SN74H10N	
U 28	1	046-97-00138		IC,LIN COMPTR,DIFF HS	TI/MML40	SN72710L	
U 29	1	046-97-00138		IC,LIN COMPTR,DIFF HS	TI/MML40	SN72710L	
U 30	1	046-97-00152		IC,STTL FF,D POS EDGE	TI/MML32	SN74S74N	
U 31	1	046-97-00115		IC,HTTL GATE,NAND 3-INP	TI/MML32	SN74H10N	
U 32	1	046-97-00168		IC,STTL FF,J-K NEG EDGE	TI/MML32	SN74S113N	
U 33	1	046-97-00046		IC,TTL GATE,NOR 2-INP	TI/MML32	SN7402N	
U 34	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 35	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 36	1	046-97-00160		IC,TTL OSMV,RETRIG	TI/MML32	SN74123N	* K
REF 1	1	905-01-00974	23877	SCHEM,PWA,CODE CONVERTER	EMR	905-01-00974	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 23885 REV DATE 01/11/75 REV LTR A

LIST TITLE PWA,OUTPUT AMPLIFIER CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-01371 ECO 51072 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00917	23884	PWB,OUTPUT AMPLIFIER	EMR	204-99-00917	
2	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
3	1	299-99-00011	6477-10	EJCTR,CARD,.062BD,POSN11	EMR	299-99-00011	
4	19	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN	100-00J-NY	
C 1	9	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
THRU							
C 9							
C 10	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 11	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR	337-14-68003	
C 12	1	337-13-10004	601	CAP.,10MF 10% 20V	EMR	337-13-10004	
C 13	1	301-13-10003		CAP,CR , 50V 1.00UF 20%	MML 48	8131-050-651-105M/MML	
CR 1	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 2	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
CR 3	1	088-99-00339	642-03	DIODE,ZENER 0.4W 4.3V	EMR	088-99-00339	
CR 6	1	088-99-00339	642-03	DIODE,ZENER 0.4W 4.3V	EMR	088-99-00339	
CR 7	14	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA	JEDEC	1N4148	
THRU							
CR 20							
Q 1	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 2	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
Q 3	5	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
THRU							
Q 7							
Q 8	5	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE	JEDEC	2N3947	
THRU							
Q 12							
Q 13	7	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V	MML 4	2N3251/2N3251A	
THRU							
Q 19							
R 1	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 2	1	616-02-47000		RES,4.7K 5% 1/4W	ALLEN BRAD	RC07GF472J	
R 3	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 4	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 5	1	616-02-47000		RES,4.7K 5% 1/4W	ALLEN BRAD	RC07GF472J	
R 6	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 7	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 8	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 9	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 10	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 11	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 12	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 13	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 14	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 15	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 16	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	

FIRST USAGE MODEL 9720-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
R 17	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 18	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 19	1	622-02-10000		RES. 1K 5% 1/2W	ALLEN BRAD	RC20GF102J	
R 20	1	616-02-15009		RES,150 OHM 5% 1/4W	ALLEN BRAD	RC07GF151J	
R 21	1	616-02-01509		RES,15 OHM 5% 1/4W	ALLEN BRAD	RC07GF150J	
R 22	4	616-02-06209		RES, 62 OHM 5% 1/4W	ALLEN BRAD	RC07GF620J	
THRU							
R 25							
R 26	1	616-02-22009		RES,2.2K 5% 1/4W	ALLEN BRAD	RC07GF222J	
R 27	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 28	1	616-02-68009		RES,680 OHM 5% 1/4W	ALLEN BRAD	RC07GF681J	
R 29	1	616-02-22000		RES,2.2K 5% 1/4W	ALLEN BRAD	RC07GF222J	
R 30	1	616-02-05109		RES,51 OHM 5% 1/4W	ALLEN BRAD	RC07GF510J	
R 31	1	616-02-68009		RES,680 OHM 5% 1/4W	ALLEN BRAD	RC07GF681J	
R 32	1	622-02-15000		RES. 1.5K 5% 1/2W	ALLEN BRAD	RC20GF152J	
R 33	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 34	1	622-02-15000		RES. 1.5K 5% 1/2W	ALLEN BRAD	RC20GF152J	
R 35	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 36	1	622-02-15000		RES. 1.5K 5% 1/2W	ALLEN BRAD	RC20GF152J	
R 37	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 38	1	622-02-15000		RES. 1.5K 5% 1/2W	ALLEN BRAD	RC20GF152J	
R 39	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 40	1	622-02-15000		RES. 1.5K 5% 1/2W	ALLEN BRAD	RC20GF152J	
R 41	1	616-02-33009		RES,330 OHM 5% 1/4W	ALLEN BRAD	RC07GF331J	
R 42	7	616-02-47000		RES,4.7K 5% 1/4W	ALLEN BRAD	RC07GF472J	
THRU							
R 48							
TP 1	3	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* Q
THRU							
TP 3							
TP 4	1	143-98-00013		JACK,TEST PT,PW TYPE,YEL	E F JOHNSON	105-0857-001	* P
TP 5	1	143-98-00011		JACK,TEST PT,PW TYPE,GRN	E F JOHNSON	105-0854-001	* P
TP 6	1	143-98-00014		JACK,TEST PT,PW TYPE,BLU	E F JOHNSON	105-0860-001	* P
TP 7	1	143-98-00015		JACK,TEST PT,PW TYPE,VIO	E F JOHNSON	105-0862-001	* P
TP 8	1	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* Q
U 1	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
U 2	1	046-97-00078		IC,HTTL GATE,NAND 2-INP	TI/MML32	SN74H00N	
REF 1	1	905-01-00968	23883	SCHEMATIC,PWA,OUTPUT AMPL	EMR	905-01-00968	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

FIRST USAGE MODEL 0720-02

E M R - T E L E M E T R Y

PARTS LIST 24326 REV DATE 03/10/77 REV LTR B

LIST TITLE PWA,REGULATOR CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-01384 ECO 54622 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
1	1	204-99-00930	24325	PWB,REGULATOR	EMR	204-99-00930	
2	3	189-98-00010		PAD,XSTR 10 PIN*USE OPTL*	MILTON ROSS	10247-N	
3	8	258-98-00002		TIE,CABLE 1/16TO 1 3/4IN	MML13	SST2S	
4	1	299-98-00002		EJECT., CARD	SCANBE	S-200	
5	1	299-99-00013	6477-12	EJCTR,CARD,.062BD,POSN13	EMR	299-99-00013	
6	8	255-98-00142		TERM.,MICRO-CLIP,PUSH-IN	VECTOR ELECT	T42-1	
7	AR	276-98-00081		WIRE,#22,STRD,WHT,600V	MML42	NAS-703-22-U-C-9	
8	AR	060-11-00019		CMPD,EPOXY,GENL PURPOSE	HYSOL	0151	
9	AR	276-99-00008	619-22	WIRE,#22,BUSS,SOLID	EMR	276-99-00008	
C 4 THRU C 6	3	337-13-10004	601	CAP., 10MF 10% 20V	EMR	337-13-10004	
C 7 THRU C 9	3	304-62-10000	600	CAP. 1000PF 1% 100V	EMR	304-62-10000	
C 12	1	339-12-15005	601	CAP., 150MF 10% 15V	EMR	339-12-15005	
C 13	1	354-64-23006		CAP, 2300UF,-10+75%, 50V	SPRAGUE/MML6	39D-238-G-050-JT-4	
C 14	1	354-64-23006		CAP, 2300UF,-10+75%, 50V	SPRAGUE/MML6	39D-238-G-050-JT-4	
C 15	1	354-70-40006		CAP., 4000MF -10&75% 25V	SPRAGUE	39D408G025JS4	
C 16	1	339-14-47004	601	CAP., 47MF 10% 35V	EMR	339-14-47004	
C 17	1	339-14-47004	601	CAP., 47MF 10% 35V	EMR	339-14-47004	
C 18 THRU C 20	3	301-13-10002		CAP,CR , 50V .100 UF 20%	MML 48	8131-050-651-104M/MML	
C 21	1	354-70-40006		CAP., 4000MF -10&75% 25V	SPRAGUE	39D408G025JS4	
CR 1 THRU CR 8	8	080-49-54010		DIO,RECTIFIER,100V 3A	WESTINGHOUSE	1N5401	
R 1	1	608-09-41200	624	RES, 4.12K 1% 1/10W	EMR	608-09-41200	* P
R 2	1	608-09-41200	624	RES, 4.12K 1% 1/10W	EMR	608-09-41200	
R 3	1	608-09-21500	624	RES. 2.15K 1% 1/10W	EMR	608-09-21500	* P
R 4	1	608-09-71500	624	RES. 7.15K 1% 1/10W	EMR	608-09-71500	* P
R 5	1	608-09-71500	624	RES. 7.15K 1% 1/10W	EMR	608-09-71500	
R 6	1	608-09-44200	624	RES. 4.42K 1% 1/10W	EMR	608-09-44200	* P
R 7	1	608-09-00000	624	RES.,*T/VAR* 1% 1/10W			
R 8	1	608-09-00000	624	RES.,*T/VAR* 1% 1/10W			
R 9	1	608-09-13700	624	RES. 1.37K OHM 1% 1/10W	EMR	608-09-13700	* P
R 10	1	628-06-00368		RES, .36 OHM 3% 3W	TEPRO	TS3W	
R 11	1	626-01-00059	621	RES, .5 OHM 3% 3W	EMR	626-01-00059	
R 12	1	628-06-00108		RES. .1 OHM 3% 3W	TEPRO	TS3W	
R 19	1	608-09-10201	624	RES, 10.2K 1% 1/10W	EMR	608-09-10201	* P
R 20	1	608-09-10201	624	RES, 10.2K 1% 1/10W	EMR	608-09-10201	
R 21	1	608-09-00000	624	RES.,*T/VAR* 1% 1/10W			
TP 1 THRU TP 4	4	143-98-00005		JACK,TEST,BLACK	MML 16	8041-1G6/MML 16	* Q

FIRST USAGE MODEL 0720-02

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION	VENDOR NAME	VENDOR PART NUMBER	USAGE
U 1 THRU U 3	3	046-97-00208		IC,LIN RGLTR,VAR,POS,37V	FCH/MML40	723HC	
REF 1	1	905-01-00984	24324	SCHEM,PWA,REGULATOR	EMR	905-01-00984	
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR	905-04-00001	

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Table 6-2. Model 720-02 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
001	CAPACITOR, 1 μF ±20%, 50V, LS.200	301-13-10002	184	2	
002	CAPACITOR, 1.0 μF ±20%, 50V, LS.20	301-13-10003	14	1	
003	CAPACITOR, 3 pF ±.5 pF, 500V	304-01-00309	11	1	
004	CAPACITOR, 10 pF ±.5 pF, 500V	304-01-01009	16	1	
005	DIODE, Ref., 9V/7.5 mA, .001%	088-10-09380	1	1	
006	DIODE, Sw., 75V/5UA, 4NS/10MA	088-10-41480	64	4	
007	DIODE, 5.1V, 1W, Sim. Std., .4W	088-10-47331	2	1	
008	DIODE, Hot Carrier 15V	088-47-00019	2	1	
009	DIODE, Rectifier, 100V, 3A	088-49-54010	8	1	
010	DIODE, Ref., 6.2V/7.5 mA	088-97-08230	1	1	
011	DIODE, Zener, 3.3V	088-99-00099	65	4	
012	DIODE, Zener, 4.7V	088-99-00109	2	1	
013	DIODE, Zener, 12.0V	088-99-00119	3	1	
014	DIODE, Zener, 5.1V	088-99-00129	1	1	
015	DIODE, Zener, 5.6V	088-99-00199	9	1	
016	DIODE, Zener, 6.2V	088-99-00329	5	1	
017	DIODE, Zener, 4.3V	088-99-00339	2	1	
018	DIODE, Zener, 9.1V	088-99-00379	1	1	
019	FILTER, Line, 1.5A, 115V AC	114-98-00072	2	1	
020	INDICATOR, LED, Red, 150 UW at 10 mA	137-97-00001	16	2	
021	INTEGRATED CIRCUIT, Pres., Decade/ Binary Counter	046-11-00035	2	1	
022	INTEGRATED CIRCUIT, Edge-Triggered Flip-Flop	046-11-00036	2	1	
023	INTEGRATED CIRCUIT, Edge-Triggered Dual J-K Flip-Flop	046-11-00037	2	1	
024	INTEGRATED CIRCUIT, 2 Trig., Mono-stable Multivibrator	046-11-00045	1	1	
025	INTEGRATED CIRCUIT, 3 Xstr. and 1 Diff.	046-15-00003	4	1	

Table 6-2 (Cont'd.). Model 720-02 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
026	INTEGRATED CIRCUIT, Phase Freq. Det.	046-16-00026	1	1	
027	INTEGRATED CIRCUIT, Dual Operational Amplifier	046-16-00028	9	1	
028	INTEGRATED CIRCUIT, Operational Amplifier, CMVIN ± 15V	046-16-00029	5	1	
029	INTEGRATED CIRCUIT, Differential Comparator	046-18-00001	3	1	
030	INTEGRATED CIRCUIT, Voltage Regulator	046-18-00020	3	1	
031	INTEGRATED CIRCUIT, Quad 2 In Pos Digital Mux	046-18-00028	11	1	
032	INTEGRATED CIRCUIT, V Comparator, Analog, H+Speed	046-33-00005	9	1	
033	INTEGRATED CIRCUIT, Operational Amplifier, 18V	046-34-00004	2	1	
034	INTEGRATED CIRCUIT, LM201AH Operational Amplifier	046-34-00009	2	1	
035	INTEGRATED CIRCUIT, Amplifier Operational, High Prem.	046-34-00017	1	1	
036	INTEGRATED CIRCUIT, High Speed Buffer	046-34-00018	9	1	
037	INTEGRATED CIRCUIT, Operational Amplifier, High Speed	046-34-00020	10	1	
038	INTEGRATED CIRCUIT, Operational Amplifier, Intl. Compen.	046-34-00021	1	1	
039	INTEGRATED CIRCUIT, Amplifier, Compensated Operational	046-45-00004	5	1	
040	INTEGRATED CIRCUIT, Quad, 2 Input Pos	046-97-00044	9	1	
041	INTEGRATED CIRCUIT, 2 In Pos Nor Gate	046-97-00046	1	1	

Table 6-2 (Cont'd.). Model 720-02 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
042	INTEGRATED CIRCUIT, Hex Inverters	046-97-00047	7	1	
043	INTEGRATED CIRCUIT, Hex Inverters	046-97-00048	6	1	
044	INTEGRATED CIRCUIT, Quad 2 In Pos AND	046-97-00049	4	1	
045	INTEGRATED CIRCUIT, Triple 3 In Pos	046-97-00050	4	1	
046	INTEGRATED CIRCUIT, Dual 4 In Pos NAND	046-97-00052	2	1	
047	INTEGRATED CIRCUIT, 8 In Pos NAND Gate	046-97-00054	2	1	
048	INTEGRATED CIRCUIT, Quad 2 In Excl-OR	046-97-00068	11	1	
049	INTEGRATED CIRCUIT, Decade Counters	046-97-00069	6	1	
050	INTEGRATED CIRCUIT, 4 Bit Binary Count.	046-97-00071	2	1	
051	INTEGRATED CIRCUIT, Monostable Multi.	046-97-00075	7	1	
052	INTEGRATED CIRCUIT, Sync 4 Bit Up/ Down	046-97-00076	1	1	
053	INTEGRATED CIRCUIT, Quad 2 In Pos NAND	046-97-00078	8	1	
054	INTEGRATED CIRCUIT, Hex Inverters	046-97-00080	5	1	
055	INTEGRATED CIRCUIT, Dual 2 Wide, 2 In	046-97-00081	2	1	
056	INTEGRATED CIRCUIT, Quad 2 Input OR Gates	046-97-00088	1	1	
057	INTEGRATED CIRCUIT, BCD/DEC, 4	046-97-00089	3	1	
058	INTEGRATED CIRCUIT, Decoder/Driver, 30V	046-97-00091	5	1	
059	INTEGRATED CIRCUIT, Decoder/Driver, 15V	046-97-00093	1	1	
060	INTEGRATED CIRCUIT, Decoder/Demux	046-97-00094	1	1	

Table 6-2 (Cont'd.). Model 720-02 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	VENDOR NAME	VENDOR PART NO.
061	INTEGRATED CIRCUIT, Data Selector/ Storage Register	046-97-00101	T.I.	SN74L98N-00
062	INTEGRATED CIRCUIT, Data Selectors	046-97-00103	T.I.	SN74151N-00
063	INTEGRATED CIRCUIT, Programmable Decade	046-97-00110	T.I.	SN74190N-00
064	INTEGRATED CIRCUIT, Programmable Binary	046-97-00111	T.I.	SN74191N-00
065	INTEGRATED CIRCUIT, Tpl. 3 Input Pos NAND Gate	046-97-00115	T.I.	SN74H10N
066	INTEGRATED CIRCUIT, AND Gate, Triple 3 Input	046-97-00119	T.I.	SN74H11N-00
067	INTEGRATED CIRCUIT, Differential Comparator	046-97-00138	T.I.	SN72710L-00
068	INTEGRATED CIRCUIT, 8 Bit, Serial Shift Register	046-97-00146	T.I.	SN74164N-00
069	INTEGRATED CIRCUIT, Flip-Flop, Dual, D-Type	046-97-00152	T.I.	SN74S74N-00
070	INTEGRATED CIRCUIT, 2-4 Input Pos NAND Gates	046-97-00161	T.I.	SN74H20N-00
071	INTEGRATED CIRCUIT, 4-2 Input NAND Gates	046-97-00162	T.I.	SN74S00N-00
072	INTEGRATED CIRCUIT, Triple 3 Input Pos AND Gates	046-97-00164	T.I.	SN74S11N-00
073	INTEGRATED CIRCUIT, Hex Inverter, Schottky	046-97-00165	T.I.	SN74S04N-00
074	INTEGRATED CIRCUIT, 8 In Pos NAND Gate	046-97-00166	T.I.	SN74H30N-00
075	INTEGRATED CIRCUIT, 2 J-K Flip-Flop, With Clear 16 Pin	046-97-00167	T.I.	SN74S112N-00
076	INTEGRATED CIRCUIT, 2 J-K Flip-Flop, Presettable	046-97-00168	T.I.	SN74S113N-00
077	INTEGRATED CIRCUIT, BCD-to-BIN Converters	046-97-00169	T.I.	SN74184N-00

Table 6-2 (Cont'd.). Model 720-02 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
078	INTEGRATED CIRCUIT, Tpl. 3 Input Pos NAND Gate	046-97-00170	4	1	
079	INTEGRATED CIRCUIT, 2-4 Input Pos NAND Gates	046-97-00171	3	1	
080	INTEGRATED CIRCUIT, Quad 2 Input Excl-OR Gate	046-97-00172	1	1	
081	INTEGRATED CIRCUIT, Data Selectors/ Mux	046-97-00176	1	1	
082	LAMP, T-1-3/4 28V, .04A	151-02-00001	1	1	
083	POTENTIOMETER, 500Ω ± 10%, 1W	201-98-00014	1	1	
084	POTENTIOMETER, 1K ± 10%, 1W	201-98-00015	2	1	
085	POTENTIOMETER, 200Ω ± 10%, 1W	201-98-00029	1	1	
086	POTENTIOMETER, 20K ± 10%, 1W	201-98-00040	1	1	
087	POTENTIOMETER, 2K ± 10%, 1W	201-98-00089	1	1	
088	POTENTIOMETER, 100Ω ± 5%, 1/2W	201-98-00210	2	1	
089	POTENTIOMETER, 1 kΩ ± 5%, 1/2W	201-98-00211	2	1	
090	POTENTIOMETER, 500Ω ± 5%, 1/2W, PC MT	201-98-00250	1	1	
091	PRINTED-WIRING ASSY., Loop Filter	205-89-01361	1	*1	
092	PRINTED-WIRING ASSY., 1st Filter Pole Pair	205-89-01362	1	*1	
093	PRINTED-WIRING ASSY., 2nd Filter Pole Pair	205-89-01363	1	*1	
094	PRINTED-WIRING ASSY., VCO	205-89-01364	1	*1	
095	PRINTED-WIRING ASSY., DC Restorer	205-89-01366	1	*1	
096	PRINTED-WIRING ASSY., Output Amplifier	205-89-01371	1	*1	
097	PRINTED-WIRING ASSY., Format Store	205-89-01373	1	*1	
098	PRINTED-WIRING ASSY., Code Converter	205-89-01376	1	*1	
099	PRINTED-WIRING ASSY., Filter Control	205-89-01377	1	*1	
100	PRINTED-WIRING ASSY., Source Select	205-89-01104	1	*1	

* to be spared when an MTBF of 30 minutes is a requirement.

Table 6-2. (Cont'd.). Model 720-02 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
101	PRINTED-WIRING ASSY., Bit Rate Store	205-89-01110	1	*1	
102	RECTIFIER, 100V In 70V rms Cont.	214-98-00022	1	1	
103	RELAY, 1 Form A, Rhod. Cont.	219-98-00078	5	1	
104	RESISTOR, .5Ω ± 3%, 3W	626-01-00059	1	1	
105	RESISTOR, .1Ω ± 3%, 3W	628-06-00108	1	1	
106	RESISTOR, .36Ω ± 3%, 3W	628-06-00368	1	1	
107	RESISTOR, 1150Ω ± .1%, .3W	648-53-11500	3	1	
108	RESISTOR, 1570Ω ± .1%, .3W	648-53-15700	2	1	
109	RESISTOR, 5750Ω ± .1%, .3W	648-53-57500	2	1	
110	SWITCH, PB, Lited, Altn. 2 Form Z	250-98-00044	1	1	
111	TRANSISTOR, NPN 75V, DC/UHF Ampl.	263-10-22221	1	1	
112	TRANSISTOR, NPN 60V RF Ampl., Conv.	263-10-22700	4	1	
113	TRANSISTOR, NPN LL Chopper 45V	263-10-24321	1	1	
114	TRANSISTOR, PNP LL Chopper HFE	263-10-29451	89	4	
115	TRANSISTOR, NPN 15A Sw-Ampl. 100V	263-10-30550	2	1	
116	TRANSISTOR, PNP, Sw/Ampl., 50V	263-10-32510	24	2	
117	TRANSISTOR, NPN 40V Sw-Ampl., HFE	263-10-39470	20	2	
118	TRANSISTOR, NPN VHF Converters	263-10-51790	1	1	
119	TRANSISTOR	263-15-22700	1	1	
120	TRANSISTOR, NPN, Dual, Diff. Ampl.	263-16-00234	1	1	
121	TRANSISTOR, NPN, Darlington To-3	263-16-40330	1	1	
122	TRANSISTOR, Matched Set	263-92-00089	1	1	
123	TRANSISTOR, NPN 20V Sw., 350 MHz	263-99-00099	2	1	
124	VACTROL, Cur. Rglt. Res., DK50Ω	101-98-00002	11	1	

* to be spared when an MTBF of 30 minutes is a requirement.